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OLLSCOIL NA HÉIREANN, CORCAIGH
NATIONAL UNIVERSITY OF IRELAND, CORK



**CONFORMAL AND NON-DESTRUCTIVE DOPING
TOWARDS GATE-ALL-AROUND NANOWIRE
DEVICES**

THESIS PRESENTED BY

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FOR THE DEGREE OF

M.ENG.SC

UNIVERSITY COLLEGE CORK

SCHOOL OF ELECTRICAL ENGINEERING

TYNDALL NATIONAL INSTITUTE

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This is to certify that the work I am submitting is my own and has not been submitted for another degree, either at University College Cork or elsewhere. All external references and sources are clearly acknowledged and identified within the contents. I have read and understood the regulations of University College Cork concerning plagiarism.

Fintan Meaney

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LIST OF ABBREVIATIONS

1D	One Dimensional
2D	Two Dimensional
3D	Three Dimensional
μ -4PP	Micro Four Point Probe
ADP	Allyldiphenylphosphine
AFM	Atomic force Microscopy
As Rec	As Received
BOE	Buffered Oxide Etchant
CMOS	Complementary Metal Oxide Semiconductor
CTLM	Circular Transfer Length Method
DIBL	Drain-Induced Barrier-Lowering
DoS	Density of States
EBL	Electron Beam Lithography
ECV	Electrochemical Capacitance Voltage
EDX	Energy-dispersive X-ray spectroscopy
ERDF	European Regional Development Fund
FET	Field Effect Transistor
FinFET	Fin Field effect Transistor
GAA	Gate All Around
HAADF	High Angle Annular Dark Field
HF	Hydrofluoric Acid
high-k	High Dielectric Constant
HMDS	hexamethyldisilazane
HRTEM	High Resolution Transmission Electron Microscope
HSQ	Hydrogen Silsesquioxane
ICP	Inductively Coupled Plasma
I/O	Input / Output
I-V	Current-Voltage
IPA	Isopropyl Alcohol
IRDS	International Roadmap for Devices and Systems
LTA	Laser Thermal Anneal
n-MOS	n-Type Metal Oxide Semiconductor
NVM	Non-Volatile Memory
MLD	Monolayer Doping
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MOVPE	Metal Organic Vapour Phase Epitaxy
p-MOS	p-Type Metal Oxide Semiconductor
RF	Radio Frequency
RIE	Reactive Ion Etch
RMS	Root Mean Squared
R_{sd}	Source-Drain Series Resistance
RTA	Rapid Thermal Anneal
SEM	Scanning Electron Microscopy
SLM	Standard Litres per Minute
SSRM	Scanning Spreading Resistance Microscopy

STEM	Scanning Transmission Electron Microscopy
Si	Silicon
SIMS	Secondary Ion Mass Spectrometry
SOD	Spin on doping
SOI	Silicon on insulator
SPER	Solid Phase Epitaxial Recrystallization
SRAM	Static Random Access Memory
TBA	Tertiarybutylarsine
TED	Transient Enhanced Diffusion
TEM	Transmission Electron Microscopy
USJ	Ultra Shallow Junction
UV	Ultraviolet
XTEM	Cross Sectional Transmission Electron Microscopy
XSTEM	Cross Sectional Scanning Transmission Electron Microscopy

Candidates Contributions

Sample processing and characterisation during this project was a joint effort of myself and other member of Tyndall and UCC.

Interpretation of results and experimental planning was a joint effort of all members of the CONDUCT2 project, with insight from collaborators both internal and external.

Any work completed outside of Tyndall/UCC is clearly stated within the text.

Thesis creation was primarily my responsibility, with crucial editing and suggestion for colleagues.

Abstract

Due to the approach of fundamental 2D topological limits, scaling of silicon transistors towards GAA devices will be required.

This thesis will discuss why continued scaling towards GAA devices will require novel doping processes and suggest possible technologies to suit this application.

Chapter 1 will detail an introduction to this topic and discuss current possible solution to 3D doping as well as explain some of the different techniques uses throughout the work

Chapter 2 discusses gas phase doping as a promising candidate as it has a superior ability to conformally dope tight 3D architectures, when compared to ion implantation. This process needs to be optimised to find a balance between the potential to etch on one hand and deposit potentially unwanted layers on the other. Further work currently ongoing to limit the thermal budget of these process will also play a critical role in their applications in modern semiconductor processing where temperature sensitive materials are ever more present.

Chapter 3 presents a one step process that simplifies traditional ion implantation while also displaying a possible route toward high levels of activation at lower temperatures. The electrical characterisation of these devices will show how this process needs further optimisation to reach conductivity levels required for GAA transistors.

Chapter 1: INTRODUCTION

1.1 MOTIVATION AND BACKGROUND

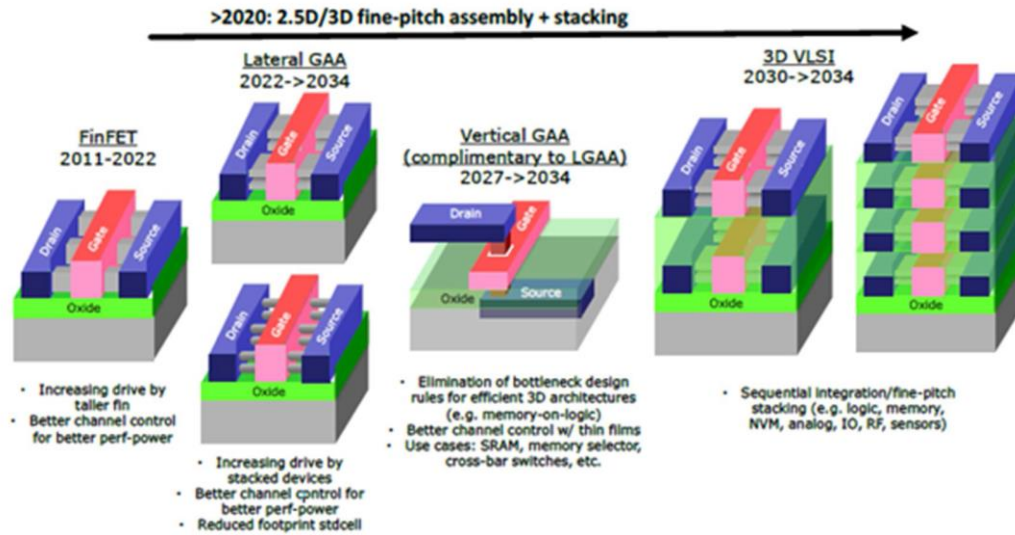
The semiconductor industry has matched the pace of that predicted by Moore's Law for over 50 years, doubling the number of transistors every two years on average¹. As a consequence, as transistors became smaller, they could also be switched from the off to the on state at faster rates while simultaneously they became cheaper to manufacture.

Fundamental 2D topological limits have been threatening the ability of the semiconductor industry to continue scaling at these historical rates. The FinFET structure was developed to provide better electrostatic control of properties such as subthreshold leakage and saturation current over planar devices while permitting the use of sufficient device current drive. However, as the advanced silicon patterning technologies are shrinking devices down to a 5 nm technology node and below, subthreshold leakage and drain-induced barrier-lowering (DIBL) are imposing the need for a new type of MOSFET. GAA field effect transistors are shown to be the potential candidates for these advanced nodes, due to the presence of the gate on all sides of the channel. This allows even greater electrostatic control than that offered by FinFET architectures.

Shown in Figure 1, the international roadmap for devices and system (IRDS) 2018 update anticipates FinFET production is likely to sustain until 2025². Beyond 2022 a transition to GAA devices is expected to begin, potentially for 3D hybrid memory-on-logic applications. After 2031 there is no longer room for 2D geometry scaling, where 3D stacking/integration will be the driving force for the continuation of scaling. This is due to performance decreases from scaling beyond this point counteracting any perceived benefits of device scaling. Benefits of scaling channel length below 12 nm would be counteracted by

negative electrostatics, while gate pitch scaling would therefore saturate around 40 nm, allowing enough room for two 14 nm contacts necessary to keep contact resistance to an acceptable level. For the vertical GAA (projected advent ~2027), physical gate length scaling could be relaxed as the gate length is measured in the vertical direction with respect to the substrate instead of contributing to the device 2D footprint. But the advantage of this is constrained by the power penalty as a result of the increase in the channel capacitance due to increased gate lengths. After ~2031 it is theorised 2D scaling will have run out of its bag of tricks. If scaling is to continue 3D geometries must be considered.

Continuation of scaling is for the most part achieved through the optimization of established processing techniques. The advantages of this continual optimisation are obvious as it allows the production of more advanced devices without the need to reinvent the wheel. This premise has been a roadblock for technologies which have shown potential advantages over current methods, requiring these technologies not only to be advantageous to current methods but generally to address some unassailable bottlenecks in current methodologies.

Figure 1 IRDS MOSFET Predicted Timeline²

1.2 SILICON DOPING

One such bottleneck, predicted to limit the scaling of devices, is the requirement to conformally and non-destructively dope sub 10 nm 3D Gate All Around (GAA) devices. Traditionally ion implantation is used to dope devices. This process rapidly accelerates single ions of dopant and “implants” the devices with these ions. This process has many advantages such as high level of control over dopant dose and concentration, high level of control over the depth of dopant atoms, and relatively low process complexity. A major challenge for GAA devices is the increase in parasitic effects as the nanowire dimensions are scaled³. This results in large part from the difficulty to achieve a high active dopant concentration while maintaining junction abruptness in such a small three-dimensional (3D) Si area. Optimising device resistance requires high levels of control over dopant incorporation, diffusion and activation.

Ion implant has disadvantages for the doping of sub 10 nm GAA devices. Some of these are damage caused to the semiconductor crystal caused by ion bombardment and an inability to dope outside the line of sight on the ion beam. These problems are manageable in larger, planar devices however for scaled GAA devices the percentage of the device crystal that is damaged

increases and may be difficult to anneal out, and when GAA devices are stacked accessing the devices with the beam becomes difficult due to shadowing.

1.2.1 **Implant Damage**

One of the issues for the future use of ion implantation in the semiconductor industry is the surface damage to crystalline Si caused by the implantation process itself⁴. Ion implantation dopes materials by accelerating a beam of the dopant ions at a target, giving the ions enough kinetic energy to embed themselves in the target material. In the case of crystalline materials, this addition of dopant ions causes physical damage to the crystal lattice. The kinetic energy allows the ions to break the surface of the crystal, colliding with atoms deeper within the crystal until the ions lose their momentum through collision. The ions then come to rest within the substrate crystal. During this process, the destructive force supplied by the ions creates silicon vacancies and interstitials within the crystal. These silicon defects change the electronic properties of the crystal, such as conductivity and mobility. Coupled with this, the dopant ions are only electrically active when they substitutionally dope the silicon crystal. If the dopant ion is not sitting in a crystal lattice location, it is said to be inactive and does not contribute to the electronic properties of the substrate.

Currently in industry, substrates are annealed after ion implantation in an attempt to repair damage caused to the crystalline silicon by the implantation process and give the dopant ions sufficient energy to find a substitutional location within the crystal, electrically activating the dopants to give the required electrical properties.

The damage caused by ion implant is often extensive enough that the subsequent annealing step does not remove all crystal defects and instead defects evolve from simple point defects into $\{311\}$ rod-like defects and eventually into dislocation loops, or as in Figure 3 of an ion implanted fin⁵, into twin boundary or stacking fault type defects.

Annealing the substrate can also drive the dopant ions deeper into the sample, which is an unwanted effect when trying to generate ultra-shallow junctions (USJs) necessary for modern transistor devices. Post-implantation annealing is also affected by transient-enhanced diffusion (TED). TED is an effect still under investigation, where it is thought that the large excess of crystal defects like vacancies or interstitials increases the dopant's ability to locally diffuse, leading to a broader junction than classical interpretations would predict⁶⁻⁸. Additionally, as transistors scale down, these process issues become more significant, and have become a limiting factor to device performance. Implant amorphisation in 3D silicon devices can be more detrimental than would be expected in planar devices. It is proposed that this is due to the fact that in planar devices there is a very large amount of silicon that the device silicon area can seed from opposed to a geometrically isolated fin which has to recrystallize from a damaged or absent seed. This leads to a defect rich or polycrystalline device area and a corresponding increase in source-drain series resistance (R_{sd}) shown in Figure 3⁹⁻¹¹.

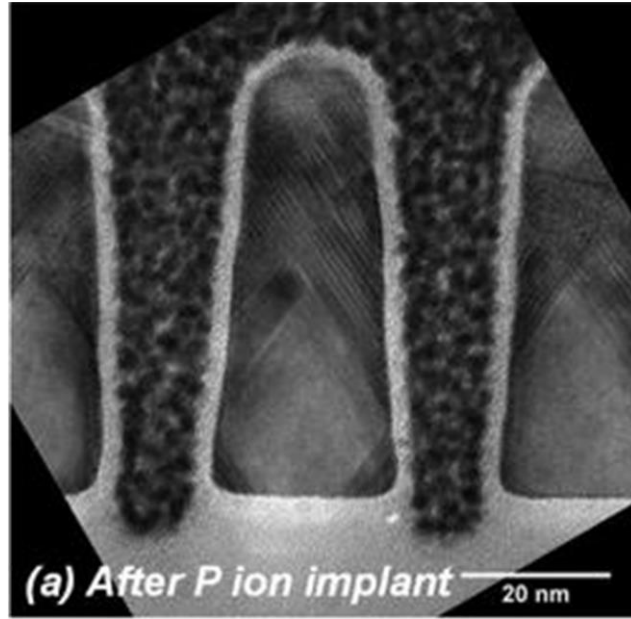


Figure 2 TEM images taken after implantation and RTA of a Si nanowire. The phosphorus implantation was performed at room temperature at 45° tilts left and right. Twin boundary defects are still evident post RTA likely to affect electrical behaviour⁵

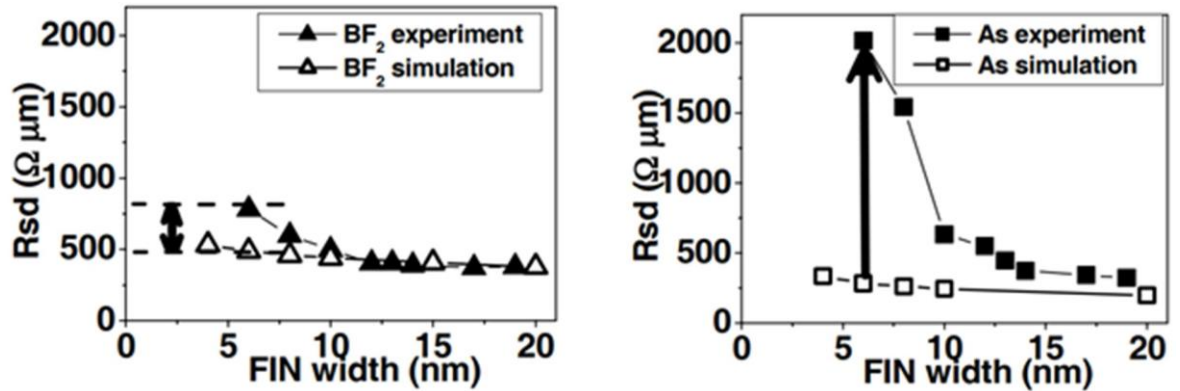


Figure 3 Rsd vs. fin width for pMOS FinFETs with a) BF₂ self-amorphising extension implants and b) As self-amorphising extension implants. Simulations match experiments for Fins wider than 10nm. Below 10nm, a clear deviation is observed believe to be caused by poor recrystallization due to a large area of the device amorphizing. pMOS FETs were affected less as the implant was less amorphizing¹¹

1.2.2 Alternative Doping Strategies

One method investigated to tackle issues with ion implantation for GAA devices, was to test other methods of introducing silicon dopants.

1.2.2.1 Gas Phase Doping

Gas-phase doping was tested as a 3D silicon device doping method. Unlike ion implantation, gas-doping is not beamline limited. Gas doping can be a conformal method, as the gas has equal access to all surfaces of the Si device. This contrasts with ion implantation, which is a line-of-sight limited. GAA devices can suffer severe shadowing effects when using ion implantation, as the device topography and vertical stacking limits the effective doping of devices. Gas-phased doping was tested for uniformity of dopant deposition in 3D geometries during this project, to overcome this current bottleneck.

Gas phase doping was also investigated with respect to silicon surface damage caused by the doping process. A well-studied issue is damage to the silicon crystal caused by physical ion implantation. As devices scale down, the effects of crystal damage become more severe, and can become a limiting factor in device manufacturing^{12,13}. Gas-phase doping is being investigated as a damage-free method of introducing dopants to Si devices. This is necessary in industry as all Si damage in manufacturing can lead to irregularities or failures in device performance and introduces uncertainty to the production yield.

1.2.2.2 Spin on Doping

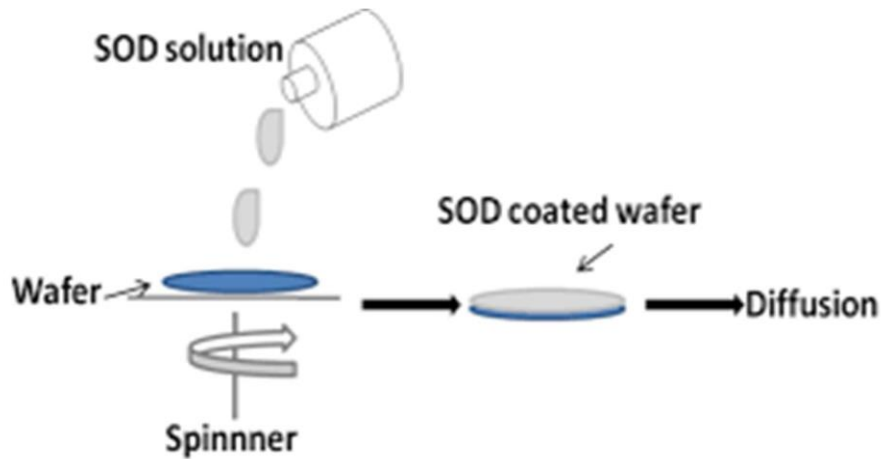


Figure 4 Spin on doping process. A mixture of a solution of SiO₂ and dopant containing molecule is dispensed on the wafer and spun to distribute. The wafer is then subjected to a high temperature anneal to drive in and activate the dopant¹⁴

Spin on-doping (SOD) is a process where dopant containing solution is spun onto the substrates, which is followed by an RTA step where the dopants diffuse into the substrate. The dopant-containing solution comprises a mixture of SiO₂ (glass) in solution and dopant molecule which is why the process can also be called spin-on-glass (SOG). SiO₂ solutions are typically used as they can be readily formed, resist high annealing temperature, and theoretically removed using standard semiconductor processing.

Advantages of SOD are process simplicity, low toxicity, low cost, and no explicit substrate damage this has historically made the process attractive to solar cell manufacturing where wafer cost is of utmost importance^{15,16}. However, these dopant containing glasses are sometimes not easily removed as the high concentration of dopant molecules inhibit the etching of the SiO₂ using standard HF chemistries. This can lead to damage to the substrate if more aggressive chemistries are used or residues if the SOD is not completely removed. SOD also suffers from conformity issues when dealing with high aspect ratio or 3D devices.

1.2.2.3 Plasma Doping

Plasma doping is where a Si wafer was directly immersed in plasma containing doping species. Most applications of plasma doping are to form an ultra-shallow junction (USJ)^{17,18}. This is due to advantages Plasma doping has over ion implantation, as by immersing the samples in a dopant containing plasma the issues surrounding low energy implants such as low ion flux can be avoided. However, contamination is sometimes an issue with plasma implantation when compared to ion implantation¹⁹. Substrate bias is used to accelerate and implant the ions into the sample this can lead to similar issues as with ion implantation such as directionally and therefore lack of conformity and damage induced by ion implantation²⁰. Generally, a high temperature anneal is performed post plasma immersion to anneal out the damage caused and activate the dopants.

1.2.2.4 Monolayer Doping

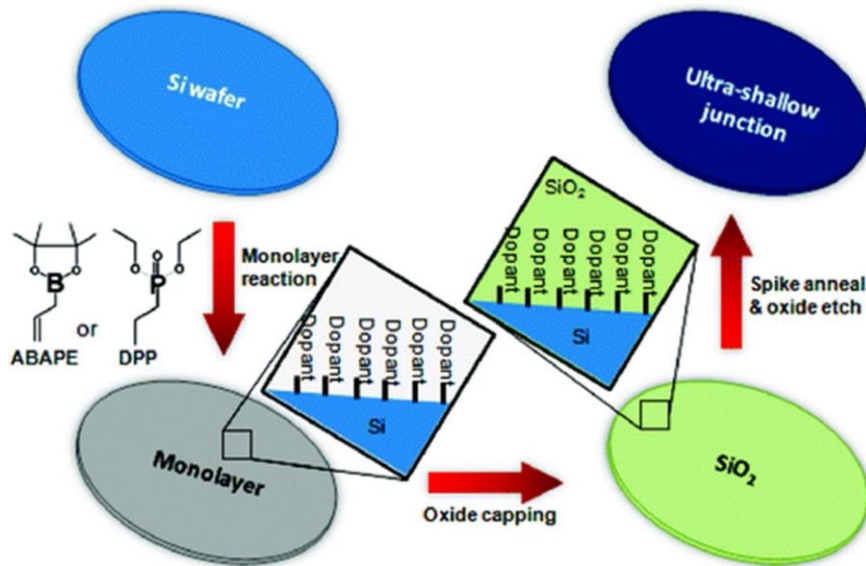


Figure 5 MLD Process. The sample is degreased, then a monolayer of the molecule that contains the target dopant is attached to the surface of the sample. A capping layer is applied to encapsulate the dopant containing monolayer and prevent it from volatilising during the high temperature anneal.²¹

MLD involves the use of wet chemistry to dope the substrate. The primary method of doping silicon using MLD involves the hydrosilylation reaction. This reaction covalently bonds an organic dopant molecule to a hydrogen-terminated silicon surface prepared by etching the native silicon oxide and h-terminating the surface with a HF treatment. MLD typically then requires a capping layer to prevent volatilisation of the dopant molecule during the high temperature annealing step used to drive in and activate the dopants.

MLD has the advantage of being potentially conformal, damage free, and highly controlled. However, MLD still suffers from an inability to get dopant dose required for source and drain implants in transistors where it's potential to create damage free USJ is of most interest.

1.2.3 Alternative Annealing Strategies

1.2.3.1 Spike RTA

Spike annealing is similar to that of furnace annealing in that it used conventional means of heating to achieve activation and diffusion of dopants. The difference is in the ramp rate of the temperature with modern spike anneals is much higher ($>400^{\circ}\text{C/s}$) than that of conventional processing allowing less time at peak temperatures and reducing diffusion. The issue with this is being able to both have high ramp rates but also get high control over the peak temperature and ramp rate enabling junction doping control²². This high ramp annealing also causes massive thermal strain on the wafer and can lead to wafer breakages.

1.2.3.2 Laser Thermal Anneal (LTA)

Laser thermal annealing involves using laser pulses to locally melt the silicon and incorporate dopants and then the silicon recrystallizes as it solidifies. Dopant activation in this way can be effectively diffusion-less and incorporation greater than that of the solid solubility can be achieved in the liquid phase. However, this process has some important integration issues as it can cause deformation of materials that have melting points below that of silicon that don't recrystallize in the same way silicon does. Materials with different light adsorption properties will also lead to cross wafer temperature variations that can build stress and lead to wafer breakages²³. Metastable materials could also potentially revert to more stable forms under the energy supplied from the laser.

1.2.3.3 Solid Phase Epitaxial Recrystallization (SPER)

Solid phase epitaxial recrystallization takes advantage of the greater rate of dopant incorporation that is seen while amorphous silicon is recrystallizing. Ion implantation is typically used to amorphise the silicon and low thermal budget recrystallization anneals ($\sim 600^{\circ}\text{C}$) can be used to recrystallize the silicon while incorporating dopants. This technique

Chapter1: Introduction

has been shown to activate dopant to metastable levels far above their solid solubility at their recrystallization temperature and can even activate dopants to similar or greater levels than that of other techniques using much higher thermal budgets. However, this metastable activation is as the same suggests quite often not stable and subsequent annealing can deactivate the dopants.²⁴

1.3 CHARACTERISATION

In the following section the analytical techniques used during the Masters project are detailed.

1.3.1 4-Point Probe Electrical Characterisation

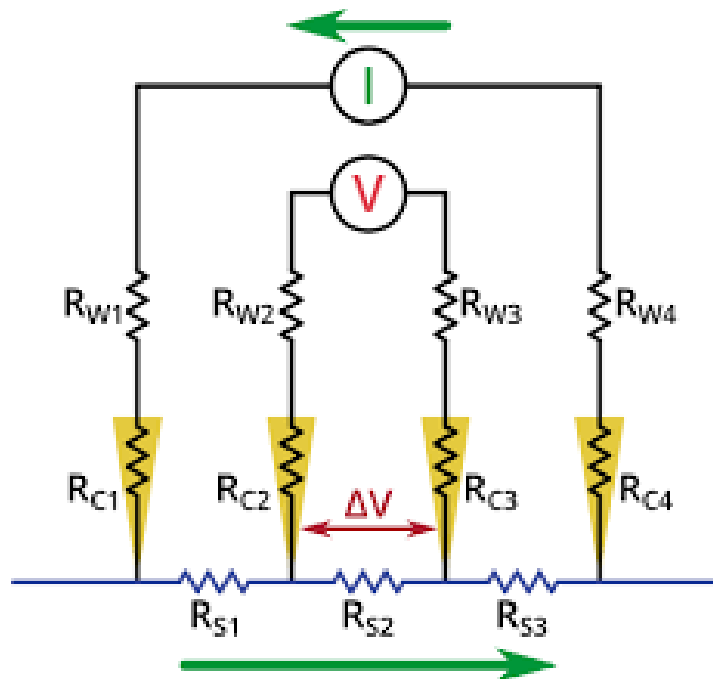


Figure 6 4-Point Probe setup. A known current is applied across the sample using the outside probes. The voltmeter shown \textcircled{V} has a very high impedance meaning practically no current flows through the two inner probe circuit. This means that the measured decrease in voltage (ΔV) is only dependant on R_{S2} (the sample resistance) impeding the flow of current. Applying ohms law resistance can be calculated trivially²⁵

The four-point probe is commonly used to measure the semiconductor resistivity. Two-point probe methods would appear to be simpler to conduct, because only two probes need to be used. But the interpretation of the measured data is more difficult. In two-point probe measurement each contact serves as a current and a voltage probe. The total measured resistance is a sum of the probe resistance, the contact resistance, and the resistance of the device. It would be very difficult to separate the resistance of the device in this test. The solution to this is the four-point probe. The current path setup is identical to that as the 2-

point probe; however, the voltage is now measured with two additional contacts. Although the voltage path still contains the probe and contact resistances, the current flowing through this path is very low due to the high input impedance of the voltmeter. The parasitic resistances are therefore negligible, and the measured resistance is dominated by that of the device of interest. In this way we can calculate the devices sheet resistance, and this can be easily converted to resistivity in confined 2D devices as with the Circular Transfer Length Method (CTLTM) devices in this study.

1.3.2 Electrochemical Capacitance Voltage (ECV)

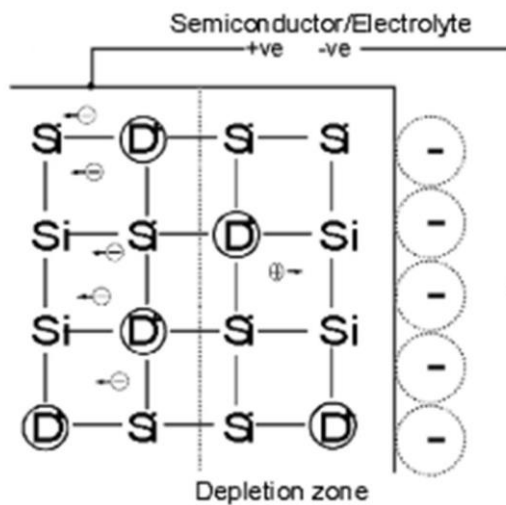


Figure 7 ECV setup for n-type semiconductor. A negative applied voltage is applied to create a depletion region by repelling donor electrons. The capacitance of this depletion region is measured to calculate carrier concentration²⁶

ECV is a tool to measure active doping profiles in semiconductors. The semiconductor sample is attached to an electrochemical cell, creating a depletion region between the sample and the electrode. The capacitance of this depletion region is measured, and information of the doping and electrically active defect densities can

be extracted from the relationship:

$$N = \frac{1}{q\epsilon_0\epsilon_r A^2} \times \frac{C^3}{\frac{dC}{dV}}$$

N = Carrier concentration

q = Electron charge

ϵ_0 = Permittivity of free space

ϵ_r = Relative permittivity of the semiconductor

A = Contact area

C = Depletion region capacitance

V = Applied voltage

Depending on the dopant type of the semiconductor, different conditions must be used to introduce positive or negative ions to the electrolyte. For p-type semiconductors (where the charge carriers are holes) positive ions are introduced via electrical current. For n-type semiconductors (charge carriers are electrons), a UV light is used to introduce a positive charge. ECV is a destructive process as etching of the semiconductor allows for depth profiling of dopants within the semiconductor device.

1.3.3 Secondary Ion Mass Spectroscopy (SIMS)

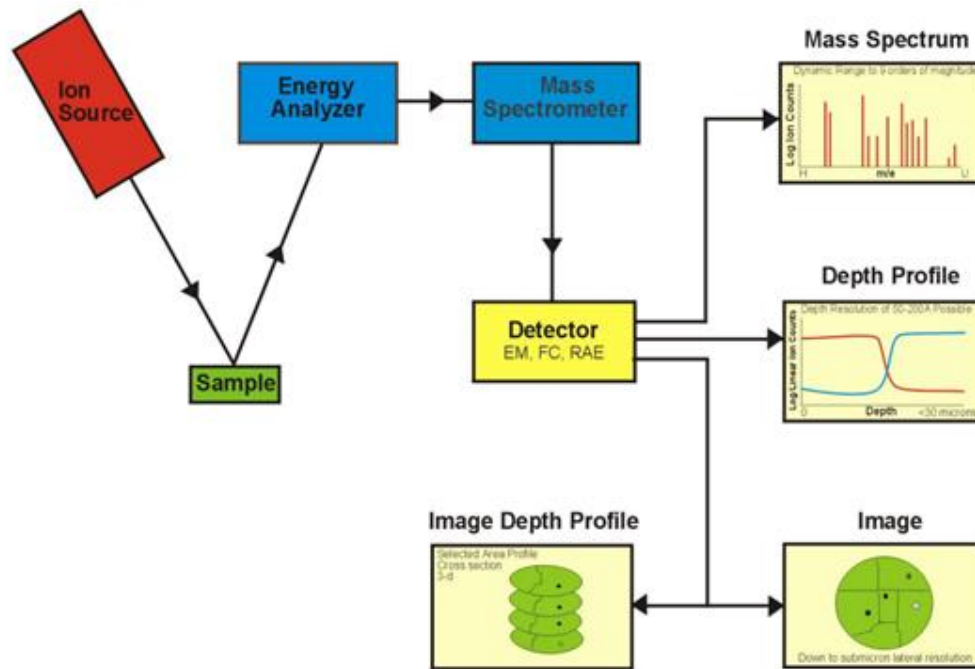


Figure 8 Schematic of a SIMS instrument.²⁷

SIMS focuses an ion source to sputter the surface of the sample by bombardment. The atoms or “secondary ions” that were sputtered are then collected, focused, filtered based on their kinetic energy in the energy analyser, and based on their mass to charge ratio at a defined kinetic energy in the mass spectrometer. Finally, the filtered ions are collected and detected and depending on the arrangement being used can be displayed in a variety of ways. Dynamic SIMS is a mode where the primary ion beam has a continuous beam of (relatively) high energy, allowing to study the ion concentration at the depths of nanometers to microns within a sample by sputtering deeper into the sample²⁸.

1.3.4 Atomic Force Microscopy (AFM)

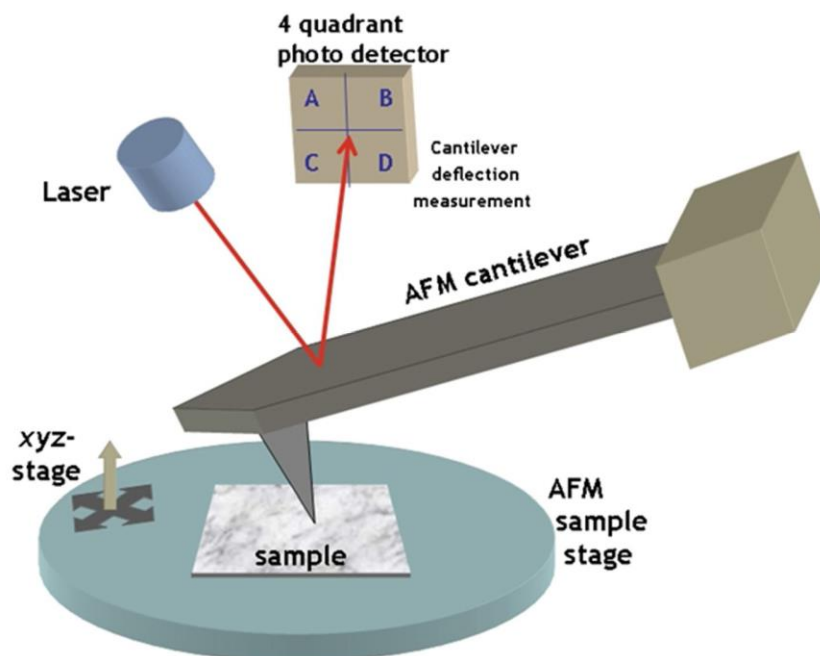


Figure 9 Atomic Force Microscope Setup.²⁹

AFM is a form of scanning probe microscopy. A cantilever with a very sharp tip is brought near or in contact with a surface, and scans over the surface using piezo control units. As the tip approaches the surface the attractive force between the surface and the tip cause the cantilever to deflect towards the surface. However, as the cantilever is brought closer to the sample the repulsive “contact” force takes over and causes the cantilever to deflect away from the surface. A laser beam focused on the cantilever is used to detect deflections towards or away from the surface. If the AFM tip passes a surface feature, the resulting cantilever deflection, and the subsequent deflection of the laser is recorded via a light sensitive detector, allowing accurate tracking of the change in height of the sample, or roughness.

Tapping mode (also known as intermittent contact mode) was used over the course of the project. The tip is driven to oscillate near its natural resonance frequency. As the tip approaches the sample surface, it interacts with the surface via non-contact forces, either Van

der Walls forces, electrostatic forces or dipole-dipole forces. This force interaction measured as a deflection on the light sensor also provides an electronic signal to the system informing it whether the cantilever height needs to be changed to be kept at a constant distance to the sample. Tapping mode was preferred as it can lessen surface damage to the sample compared to contact AFM mode. The tip is in contact with the surface for a shorter period, and with less force, leading to fewer issues with sticking of the tip on a rough surface or "gouging" of the surface if it is less hard than the tip.

1.3.5 Secondary Electron Microscopy (SEM) and Energy dispersive X-ray spectroscopy (EDX)

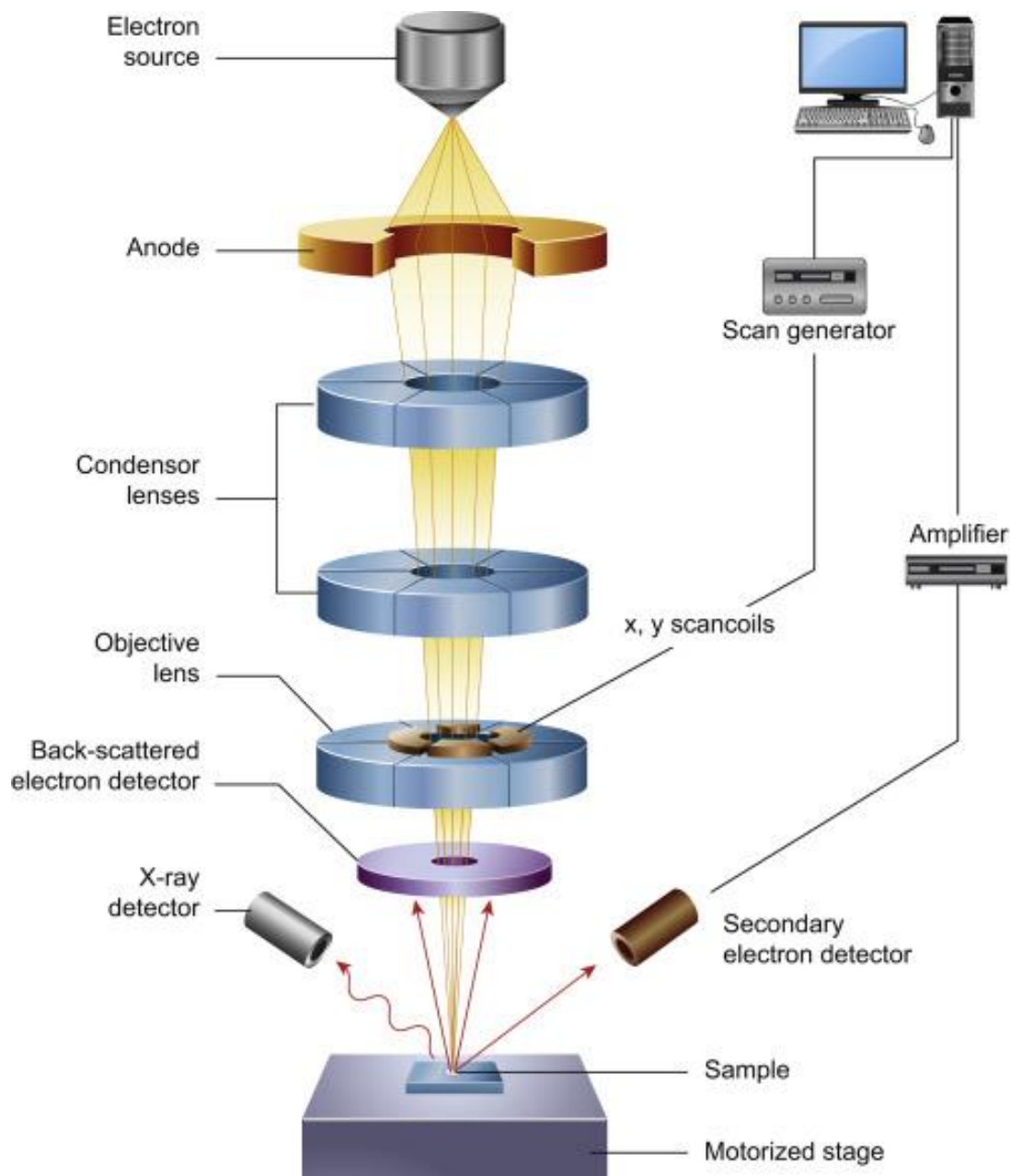


Figure 10 Cross section of a SEM setup.³⁰

SEM is an electron microscopy technique where the electron source generates electrons that are attracted to the anode and accelerated towards the sample. The beam of electrons is focused and shaped to a small circular probe on its path as it passes through the condenser lenses.

The objective lens focuses the beam on the sample while the scanning coils raster the beam over the sample. The beam interacts with the sample resulting in secondary electron produced from the sample surface containing topographical information. The secondary electrons are released from atoms in the sample which were excited by the electron beam. SEM was used in this project to get overview images of fabricated nanowires and CTLM devices and a higher resolution compared to conventional light microscopy images. Secondary electrons are generated close to the surface of the sample (few nanometres below the surface), thus contains a lot of information on the surface quality of devices imaged³¹.

In EDX imaging as the electrons scan the sample, energy is absorbed by the sample, exciting the electrons. This energy is then re-emitted as characteristic x-rays when the electrons drop back to their ground state. An x-ray detector measures the energy and number of x-rays emitted. The energy of the x-ray is a unique characteristic to the change in energy shells of the element in which the x-ray was produced. This allows the generation of an elemental composition of the sample surface.

1.3.6 Transmission Electron Microscopy (TEM) and EDX

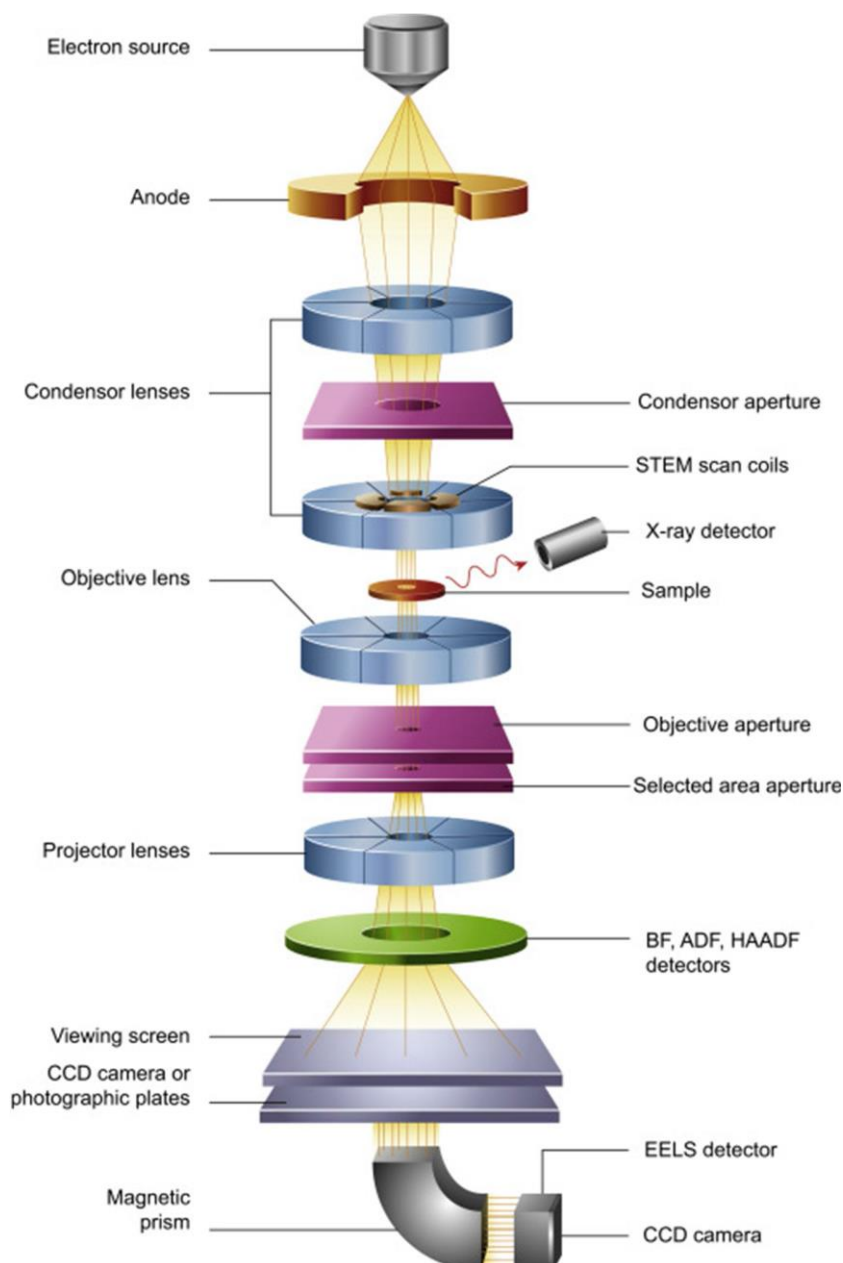


Figure 11 Cross section of a TEM setup³⁰

TEM is a form of microscopy where an electric field directs an electron beam onto a thin sample, with nanometre scale precision. The electron source generates electrons that are attracted to the anode and accelerated towards the sample. The beam of electrons is focused and shaped to a small circular probe on its path as it passes

through the condenser system. In STEM imaging mode as in SEM the scanning coils scan the beam over the sample. The beam is then transmitted through the sample and the resulting through beam is focused using the objective system on the detectors. An image of the sample's atomic structure can, therefore, undergo construction through the information gathered from the electrons³².

For EDX as in SEM the x-rays are collected near the sample, along with the imaging information this can be used for elemental mapping. Also shown in Figure 11 is an EELS detector which gathers information about electrons that interacted with the sample losing kinetic energy, which again can be linked to various information about the sample. Not shown in Figure 11 are the aberration correctors and monochromator used to obtain higher spatial and energy resolution respectively. This is a simplified explanation of a TEM, which can come in several different forms, using different electron beams and configurations to gather different information about a sample.

Scanning transmission electron microscopy (STEM) is a form of TEM which can also reach a high resolution, sometimes even higher than high resolution TEM. For STEM, the electron beam is passed through a condenser system to make an electron probe that can vary in diameter size from 0.1-10 nm³³. This probe is then scanned over the sample so that the probe passes through the rows of atoms. The STEM setting has advantages over the conventional TEM of being able, apart from reaching a very high resolution, able to record secondary and backscattered electrons and being very useful in analytical microscopy. STEM mode is used for EDX (energy dispersive x-ray spectroscopy), which was used during the project. Since a scanning electron probe is used in STEM-EDX, the location of each characteristic X-Ray source is known, allowing elemental maps to be built of the sample. EDX in TEM has some

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advantages over its use in SEM with higher beam energy 300 kV TEM beam energy allowing excitation of emission lines not possible at 30 kV used in SEM and increasing x-ray count numbers allowing qualification of elements with otherwise overlapping peaks and quantification of composition at lower atomic percentages.

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Chapter 2: TERTIARYBUTY- LARSINE DAMAGE-FREE THIN-FILM DOPING AND CONFORMAL SURFACE COVERAGE OF SUBSTRATE- RELEASED HORIZONTAL SI NANOWIRES

2.1 BACKGROUND AND MOTIVATION

Conformal damage-free doping is the holy grail for 3D semiconductor device structures, such as those used in multi-gate and nanowire-based field effect transistors (FETs). The shape, dimension, pitch, and spacing of parallel conduction paths introduce increased complexity in a number of ways, but particularly in the area of intentional impurity introduction for doping. To this end, gas-phase doping using tertiarybutylarsine (TBA) was employed to dope silicon-on-insulator (SOI) thin films based circular transfer length measurement (CTLTM) devices. Damage-free doping processes are desirable as crystal defects or surface roughness can, not only, negatively impact individual transistor device performance, but can also introduce an uncontrolled variability among devices. A conformal process implies access to all surfaces equally in order to, in this case, uniformly and reliably modify the material. Uniformity is necessary as it reduces local resistance variation which again can lead to poor electrical behaviour. As we transition to Gate-All-Around (GAA) device architectures,³⁴⁻³⁶ where all sides of the semiconductor are accessible in theory, having processes that can demonstrate access to the bottom surface are becoming increasingly sought after.

Gas-phase doping has the potential to be less damaging to the crystal structure than that of beamline implant³⁷. As Si devices scale, the effect of beamline induced crystal damage compounds as a greater percentage of the device's area will consist of damaged crystal³⁸. Beamline induced surface damage will become a more prominent issue with increasing surface to volume ratios of Si devices. Sputtering of the Si surface by the ion beam is likely to become more of a limiting factor once device pitch scaling limits the acceptable implantation angles³⁹. Limitation of the beamline angles will lead to shadowing of the Si devices, and therefore asymmetrical dopant levels. With the projected advent of GAA devices, line-of-sight implantation methodologies will be unsuitable for the doping of 3D, stacked devices.

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Gas-phase doping has a greater potential than liquid phase processes to dope the increasingly complex 3D geometries of Si devices as liquid coverage can be limited by wetting. For GAA and 3D Si nanowires, more study is necessary to see how wetting of the complex surface structure would affect dopant concentration and patterning. Surface tension effects present in liquid-based processes also have the potential to damage these fragile devices⁴⁰.

The science of dopant diffusion and activation is multi-variable,⁴¹⁻⁵¹ especially in the case of arsenic in silicon⁵²⁻⁵⁶. When dealing with 3D structures the impact of surface effects becomes crucial in determining the active dopant levels. These surface effects lead to problems for dopant incorporation/activation or as gettering points where dopants pile up⁵⁷⁻⁶². Another problem with the greater exposure to the perimeter of the 3D devices is when the doping process etches the available surface severely damaging or destroying these devices.

Gas-phase doping of silicon has been reported by several groups using various sources⁶³⁻⁷³, and our recent work on gas-phase doping of silicon was performed using arsine (AsH_3) gas to dope Si nanowires⁷⁴, where suitability for doping was shown. However severe attack of Si nanowires was seen for flowrates of 50 sccm and 250 sccm, while flowrates of 10 sccm and 20 sccm showed moderate etching. It is believed that this Si attack was in part due to the etching caused by atomic hydrogen released in the cracking of arsine. Cracking of TBA is expected to release less free hydrogen⁷⁵. In this work we consider TBA as an alternative doping source to AsH_3 , for damage-free conformal doping of thin Si films and 3D device structures. Finally, Ransom et al. used TBA in a helium carrier gas to gas-phase dope Si substrates with As⁷⁶ and they showed some very promising doping profiles, however electrical device evaluation was not conducted and the processes were not applied to thin-films or 3D structures such as nanowires, which are our primary aims here.

2.2 EXPERIMENTAL

This section contains information about the fabrication of first the nanowire and then the CTLM devices.

The nanowire devices consist of multi-finger nanowires. This creates a two-pad test structure where current/voltage characteristics are measured to characterise resistance. Different mask layout designs can be used to vary nanowire width (W), length (L), and spacing (S). The metal contact pads consist of a 10 nm Ti adhesion layer with a thicker 150 nm Au layer on top. For all nanowire devices in this project, nominally undoped (100) SOI substrates were used, with a Si thickness of 66 nm and a buried SiO₂ thickness of 145 nm. The unpatterned witness pieces used for carrier profiling were standard (100) lowly doped p-type Si wafers. For nanowire processing, the SOI substrates were patterned using the Raith VOYAGER electron beam lithography (EBL) system with a beam energy of 50 keV, and the high-resolution EBL resists hydrogen silsesquioxane (HSQ, XR1541, 2%) from Dow Corning. Sample etching took place in an Oxford Instruments System 100 ICP etcher operating in Reactive Ion Etch (RIE) mode. The etch chemistry was a Cl₂/N₂ gas mixture at flows of 20 and 40 sccm, respectively, with a chamber pressure of 10 mTorr and an RF power of 80W yielding a DC bias of 220 V. These nanowire devices are released from the substrate by means of a HF vapour etch.

CTLM devices were fabricated using a bi-layer lift off technique. Nominally undoped (100) SOI substrates were used, with Si thicknesses ranging from 4.5 nm - 66 nm and a buried SiO₂ thickness of 145 nm. First samples were primed for resist by spin coating of HMDS for 1 min at 3000 rpm. This priming modifies the surface to become hydrophobic and aids the resist adhesion. After this step LOR-3A lift of resist was spun on the samples at 3000 rpm for 50 seconds. The LOR-3A then needed to be baked at 170°C for 3 minutes to drive off the solvent and harden the resist. S1805 imaging resist was then spun on at 3000 rpm and baked at 115°C for 2 minutes

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to drive off the solvent and harden the resist.

Samples were then exposed in a Karl Suss MA6 mask aligner for 4 seconds. Samples were then developed in MF-319 for 1 minute 15 seconds. Each sample was examined under an optical microscope post development. After development 10:100 Ti:Au was deposited coating the sample. Lift off was then performed by immersion in " Microposit 1165" resist remover for 2 hours. On all samples, prior to application of the doping process, samples were degreased, and native oxide was removed.

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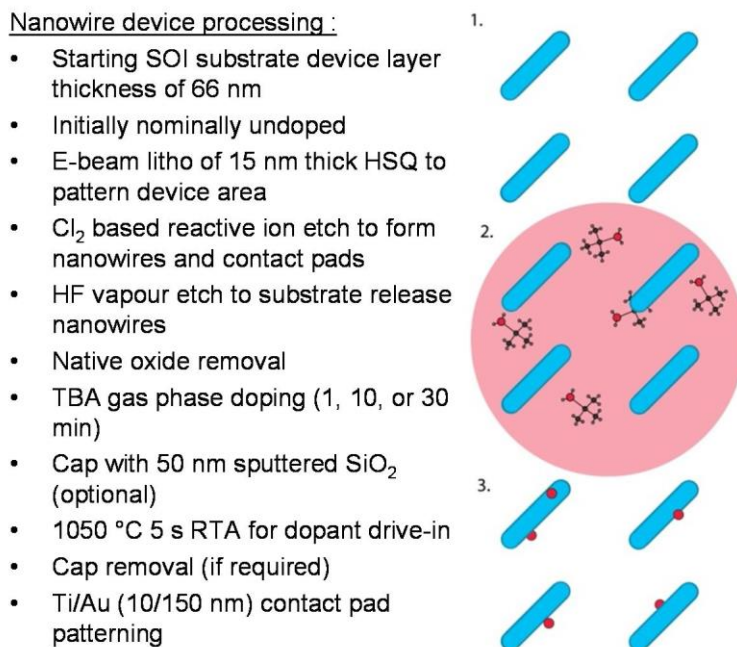


Figure 1: Process flow for nanowire formation, graphic indicates gas phase doping mechanism where arsenic containing gas is passed over nanowire devices and is cracked depositing a free arsenic layer on the surface of the devices later incorporated by rapid thermal annealing.

Gas-phase doping of all samples was carried out using a metalorganic vapour phase epitaxy (MOVPE) system. The reactor pressure was set to 700 Torr with purified hydrogen carrier gas at a flow rate of 16 standard litres per minute (SLM). Liquid tertiarybutylarsine (TBA) was used as the dopant source. Samples were heated in the reactor under hydrogen carrier gas, from 20°C to 850°C, over 15 minutes. TBA was then switched into the reactor with a controlled flow rate of 4.56×10^{-2} moles/minute and the sample were held under these conditions for 1, 10, or 30 minutes before heating was switched off. TBA was switched out of the reactor and the sample could cool to 200°C under hydrogen at a flow rate of 2 SLM. The gas was then switched to nitrogen and the sample could cool to room temperature before unloading from the reactor.

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Two separate process runs were conducted. In run 1, two bulk silicon witness pieces were processed for each of the 1, 10, and 30-minute exposure times. For each exposure time one sample had a sputtered SiO₂ capping layer prior to RTA to prevent dopant volatilisation and one did not. All samples then received a 1050°C 5 s RTA in N₂. This process run was conducted to understand the effect on dopant incorporation and sample damage that different exposures and sample capping and cap removal would have. This information was then used to decide which process would be used for run 2. For run 2 CTLM and nanowire devices and a bulk silicon witness piece, for ECV, were exposed to 1 minute of TBA with no capping layer.

Electrochemical Capacitance Voltage (ECV) profiling was performed, on the bulk Si witness pieces, to determine the electrically active carrier concentration. Before ECV profiling the capping layer, when present, was removed with a 25:1 BOE solution applied for 2 minutes 30 seconds. Ammonium bifluoride was used as the electrolyte/etchant. XTEM and EDX analysis were carried out using the FEI Titan Themis (HRTEM) operated at 300 kV in HAADF-STEM imaging mode. Cross-section samples were prepared by focused ion beam etching using a FEI's Dual Beam Helios Nanolab system. Scanning electron microscopy (SEM) was done using a Zeiss Supra 40. Electrical measurements were performed using an Agilent B1500 parameter analyser, in a Cascade manual probe system under ambient conditions.

2.3 RESULTS AND DISCUSSION

2.3.1 Dopant chemical and carrier profiling on planar samples

Figure 2 shows active carrier concentrations extracted after the process was applied to bulk substrates. In Figure 2(a) the process temperature of 850°C is sufficient to drive in and activate a certain amount of the dose. Comparing process exposure times in Figure 2(b) and Figure 2(c) exposure time had a negligible effect on active dopant concentration, suggesting the process is self-limiting.

Similar dopant levels are seen comparing Figure 2(b) and Figure 2(c) showing that the SiO₂ cap is not necessary to prevent volatilisation of the dopant molecule from the surface of the substrate and was therefore omitted on run 2. The abnormal near-surface points seen in Figure 2(c) are believed to have been caused by the ECV first profiling an arsenic rich oxide layer and then the silicon itself. This is reinforced by the observation of an arsenic rich oxide layer in STEM analysis of the nanowire devices seen in Figure 5. This effect is not seen in either the SiO₂ capped or run 2 samples, Figure 2(b) and Figure 2(d), as the removal process for the SiO₂ cap likely removed the oxide and run 2 bulk samples were therefore etched for 15 s in 25:1 BOE to prevent this ECV artefact. Comparison of the pre annealed and post annealed portions of the graph shows a different profile shape between pre-annealed and post annealed active dopant concentration. Post-annealed Si showed a Gaussian profile distribution, while pre-annealed Si showed a more exponential profile. This may be useful for Si devices where a specific dopant profile is necessary. The active concentration seen here could be redistributed by using a faster ramp rate RTA tool. Redistributing the dopant can give a higher surface concentration by limiting dopant diffusion. The RTA used in this work has a maximum ramp rate of 10°C/s giving dopant enough time to diffuse into the sample limiting the surface concentration and increasing the junction depth. With optimized annealing, diffusion could be controlled

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such that the dopant is more concentrated at the surface optimizing the profile for smaller device geometries. Subsequent runs of the process are planned to use such optimised annealing.

The unusual active profile shapes, especially seen for the longer process times are possibly linked to extreme surface roughness, which can affect the carrier profiling by ECV. This was studied in more detail by AFM.

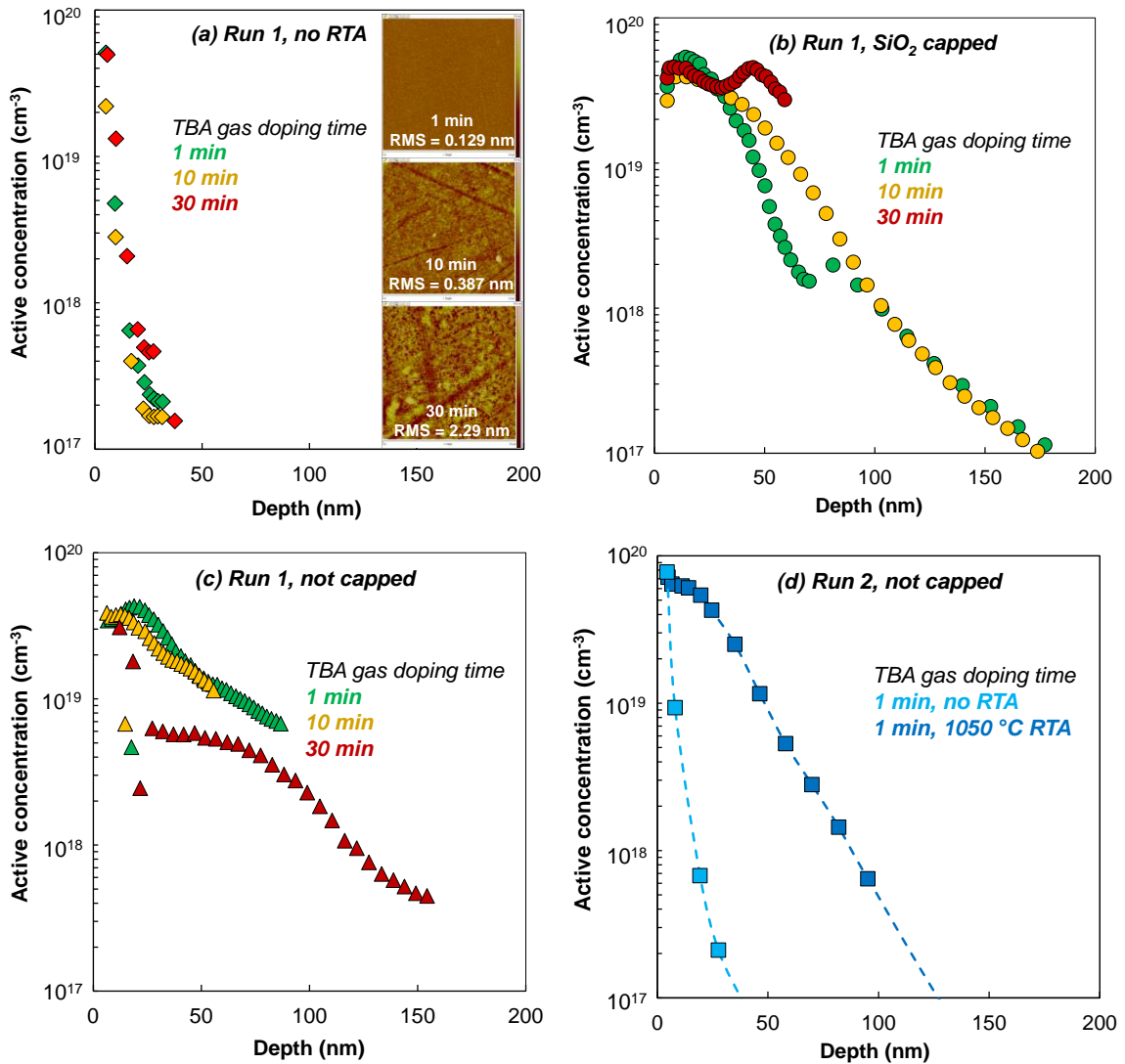


Figure 2: Representative ECV carrier profiles showing active carrier concentration. These profiles are extracted from the Si witness pieces for the process on the CTLM devices. (a) Electrically active carrier profiles extracted from process run 1 ECV conducted directly after MOVPE exposure with no post anneal. Inset: Roughness (RMS) of bulk Si witness pieces measured using AFM, RMS values are 0.129, 0.387, 2.29 nm for the 1, 10, 30 minute processes respectively. This analysis is showing clear etching of the silicon for the 10 minute and 30 minute processes. However, for the lower exposure of 1 minute the witness piece is showing no observable etching, and thus was chosen for the run 2 set of experiments. (b) Profiles extracted post 1050°C 5 s anneal on samples with SiO₂ cap. (c) Profiles extracted post 1050°C s anneal on samples without SiO₂ cap. (d) Profiles extracted both pre and post 1050°C 5 s anneal for process run 2 (applied to CTLM and nanowire devices).

Figure 2(a) shows AFM conducted on the Si witness pieces from run 1 in order to access the damage caused by the doping process. Tapping mode AFM was used, to limit probe induced damage to the surface. An RMS value of 0.129 nm for the 1 minute exposure time, shows limited to

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no etching has occurred on the surface for a low process time. In comparison, the 10 minute and 30 minute exposure times gave RMS values of 0.387 nm and 2.29 nm respectively. This shows the surface roughness increases with increased exposure to TBA gas. Since the dopant concentration has been shown to be self-limiting, keeping the exposure time short is advised to limit surface etching. It is worth noting that the AFM measurements are possibly of the conformal oxide layer on the Si surface. This means our RMS values from the AFM may not be a true indicator of the Si surface roughness. However, it is assumed that the trend in the oxide layer roughness will reflect the underlying trend of the Si surface roughness. However, we can see that both the 10 and 30 minute exposures show obvious etching of the substrate. Therefore, to reduce etching in run 2, which was applied to the CTLM and nanowire devices, a 1 minute exposure was used.

In relation to the electrical devices in this study, we have performed AFM analysis (multiple sites per sample) of the surfaces of all Si thicknesses used in this study. The surface roughness is summarised in the table below. The Si films are continuous in all cases. Overall, the roughness doesn't appear to vary significantly as we scale the Si thickness on the SOI samples, although one could argue the ratio of roughness to overall thickness is increasing. This roughness will affect the carrier scattering at the surfaces and can affect carrier mobility.

<i>SOI Thickness (nm)</i>	<i>Roughness RMS (nm)</i>
66	0.259
30	0.171
20	0.221
10.5	0.165
4.5	0.207

Figure 3: AFM roughness RMS measurements conducted on SOI thin films used for electrical characterisation.

2.3.2 Electrical characterisation of CTLM device structures

The electrical properties of the SOI samples, with Si film thickness ranging 4.5 to 66 nm, were measured using the circular transfer length method. Sets of concentric metal circular electrode pairs were deposited on the Si surface using optical lithography, metal evaporation and lift-off. The electrode metal was 100 nm thick Au on a 10 nm thick Ti adhesion layer, with electrode pair separations between 2 μm and 130 μm as described in previous work⁷⁷.

The current-voltage characteristics were measured between -1 V and +1 V and the material resistivity for each film thickness was determined by analysing the resistance with respect to electrode separation. The raw I-V data are shown in Figure 3 resistivity for each Si film thickness is presented in the inset. The material resistivity is observed to increase with decreasing film thickness, with a significant increase in resistivity at 4.5 nm. The pronounced increase in resistivity may be as a result of an undesirable doping profile in the first few nanometres of depth, or indeed low overall doping levels, which may have a more pronounced effect at thinner Si film thicknesses. Another relevant effect on the increase in resistivity is the expected sharp drop in the density of states for electron and hole conduction due to quantum confinement effects in these thin Si structures. The density of states (DoS) per unit volume for a 3D semiconductor,

a sub-10nm thin-film quantum well, and a sub-10nm quantum wire will not be the same. In effect the physical confinement produces discreteness of allowed electron energies leading to quantum effects. Moreover, the DoS could potentially drop dramatically in going from 3D to 1D, depending on the dimensions. The lower the DoS then the lower the current in the device, and hence there will be an increase in resistivity⁷⁸⁻⁸⁰.

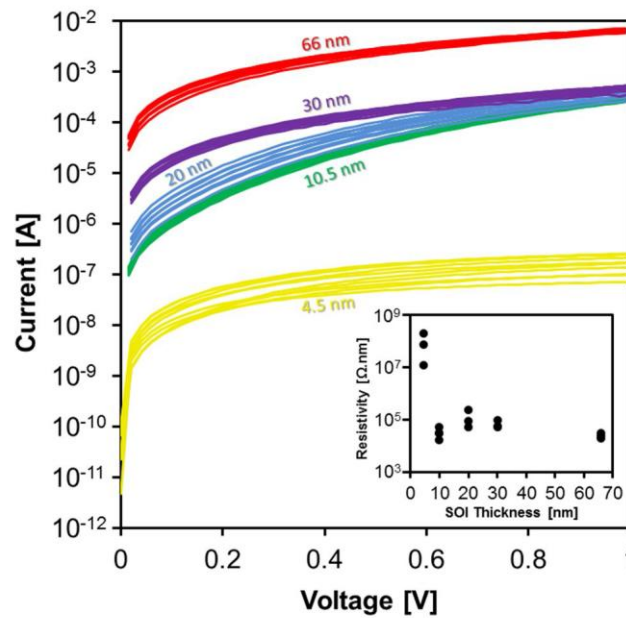


Figure 4: Representative current-voltage data from the CTLM measurements for each Si film thickness. Note these data are not normalized to thickness. Inset: Extracted resistivity values vs. Si thickness.

It should be noted that in some cases, the I-V characteristics were non-linear due to the possible presence of a Schottky barrier at the metal-Si interface. In such cases, caution is needed when attributing a single representative resistance value, from which resistivity can then be extracted. The electrode/interface/silicon can be thought of as being similar to a Schottky diode in series with a resistor, the resistance of which varies with CTLM electrode separation and is characteristic of the material under test. As such, representative resistance was determined by performing a linear regression on the current data over the voltage range of +0.75 V to +1 V

where this diode is “more switched on” and the I-V characteristics are less affected by the effects of the Schottky barrier, and more by the series resistance.

While not entirely perfect, this approach gives a more accurate determination of the series material resistance than performing a linear fit over the entire voltage range. This conclusion is based on trying to calculate the resistance of the resistor from the I-V data from the simulated diode-resistor circuit. It can be seen from Figure 5 that calculating the resistance by using data from different voltage ranges, gives different results. The full range $[-1 < V < +1]$ gives the highest error (163%) while the lowest error (5%) was achieved using the range of $[0.75 < V < 1]$. We do not claim that this method increases the accuracy of reporting the material resistance, rather it decreases the inaccuracy that would be introduced by incorporating characteristics that are dominated by the effects of the metal-Si interface.

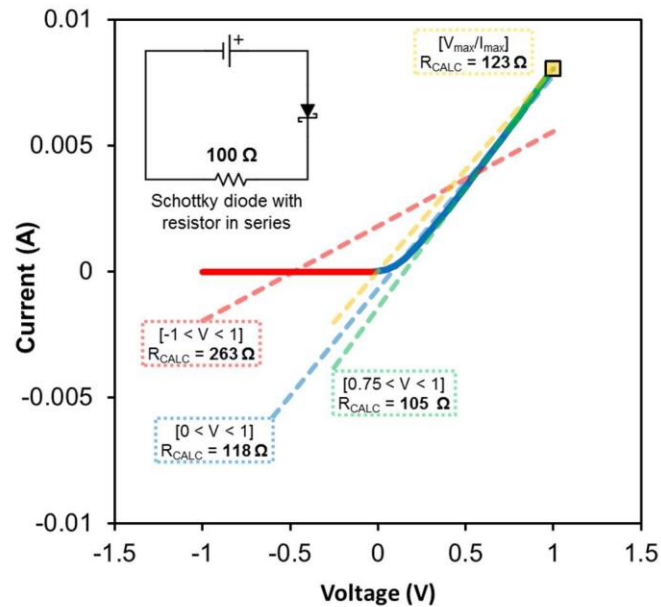


Figure 5: Simulated I-V response from the Schottky diode with series resistance circuit (inset). The trend lines and annotations display the resistance value extracted using linear regression over different voltage ranges. The actual value of the resistor used in the simulation was 100 Ω .

2.3.3 Applicability analysis for Gate-All-Around (GAA) nanowire devices

Figure 6 shows a SEM image of “4-finger” nanowires released from the substrate that also received the 1 minute TBA processing. No visible etching is noted. Figure 6 also shows a representative XSTEM of one of the nanowires, again showing no evidence of damage in the crystal structure internally in the wire or externally on the surfaces.

Line edge roughness (as a function of the lithography, etch, and subsequent processing) will be an important factor for any future electrical characterisation of these nanowires due to its effect on carrier mobility.

In future work we will be characterising the nanowire electrical behaviour and line edge roughness measurements will be included with that electrical data. An approximately 4 nm arsenic containing oxide layer, a dark grey conformal layer surrounding the light grey Si nanowire, is seen in the STEM image. EDX analysis shows the presence of arsenic in the layer. From the EDX analysis it seems like this layer is an arsenic-rich silicon oxide with little carbon

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being incorporated. This layer was also seen in the XTEM analysis of the CTLM devices (not shown). This layer may explain the non-linear behaviour seen in the electrical characterisation, as any current would have to travel through this likely semi-insulating layer.

The Si was cleaned with 2% HF for 15 s prior to the MOVPE to remove all SiO₂ from the device surface. The processing in the MOVPE reactor used highly pure gasses with no presence of O, the post-anneal was completed under N₂ not allowing the growth of oxides, and the transfer of the samples from the MOVPE to the annealing chamber was quick enough to not allow for the significant growth of an oxide conformal layer. Native oxide growth will occur in contact with ambient, and it is known that oxide growth is strongly enhanced by high carrier concentrations.⁸¹ It is more likely that the conformal oxide layer formed after the RTA. Future work will be completed to confirm when the conformal layer forms on the Si, as if the oxide forms prior to the final anneal, it may act as a limiting factor to the maximum active dopant concentration.

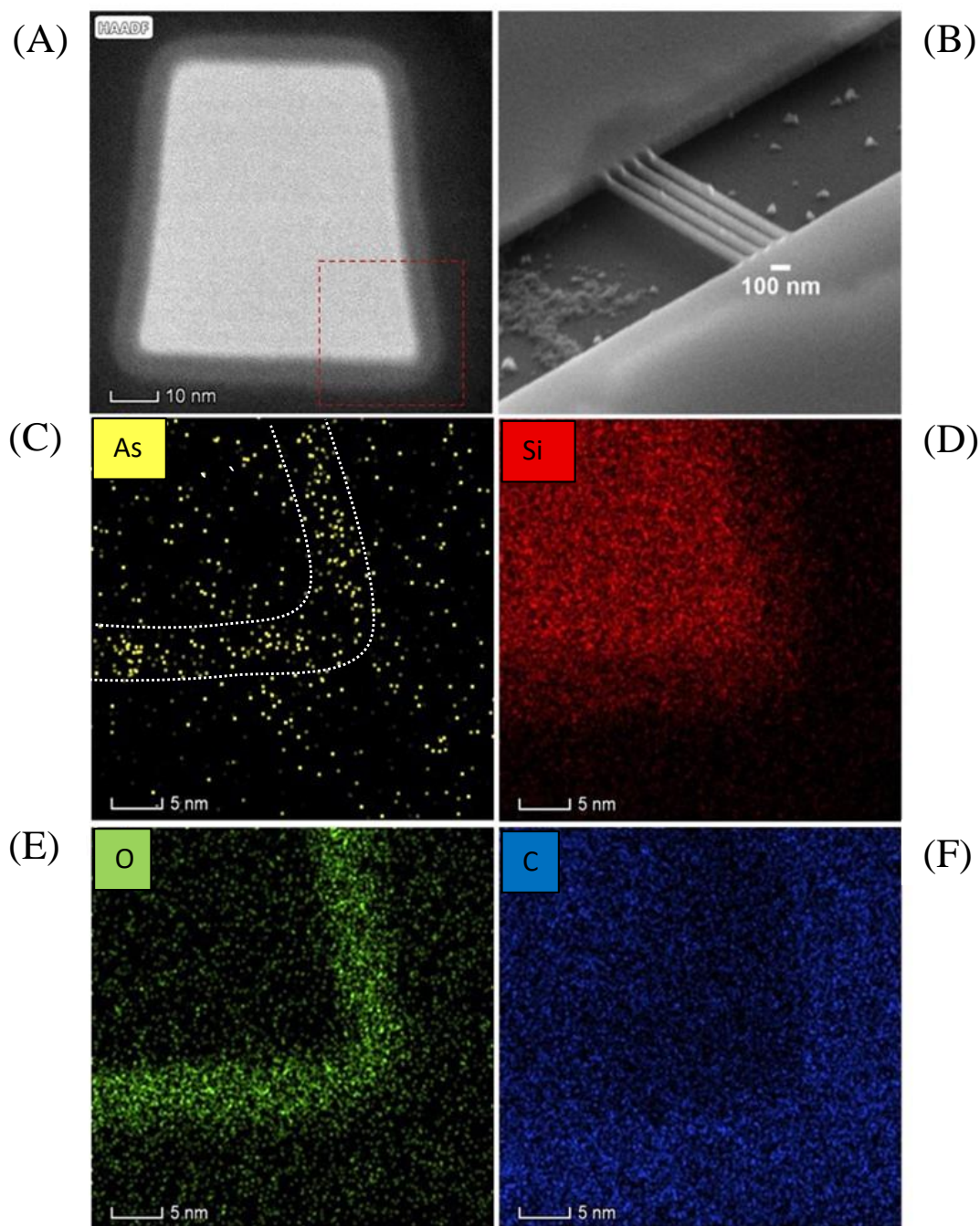


Figure 6: (A) XTEM image showing nanowire with conformal doping layer with red enclosed area indicated for EDX scan area, (B) Representative "4-finger" released nanowire device from which one nanowire was imaged, (C)-(F) EDX analysis showing presence of arsenic containing oxide layer formed (enclosed by white curves in image (C)) with minimal carbon incorporation

2.3.4 Spike anneal of TBA doped silicon

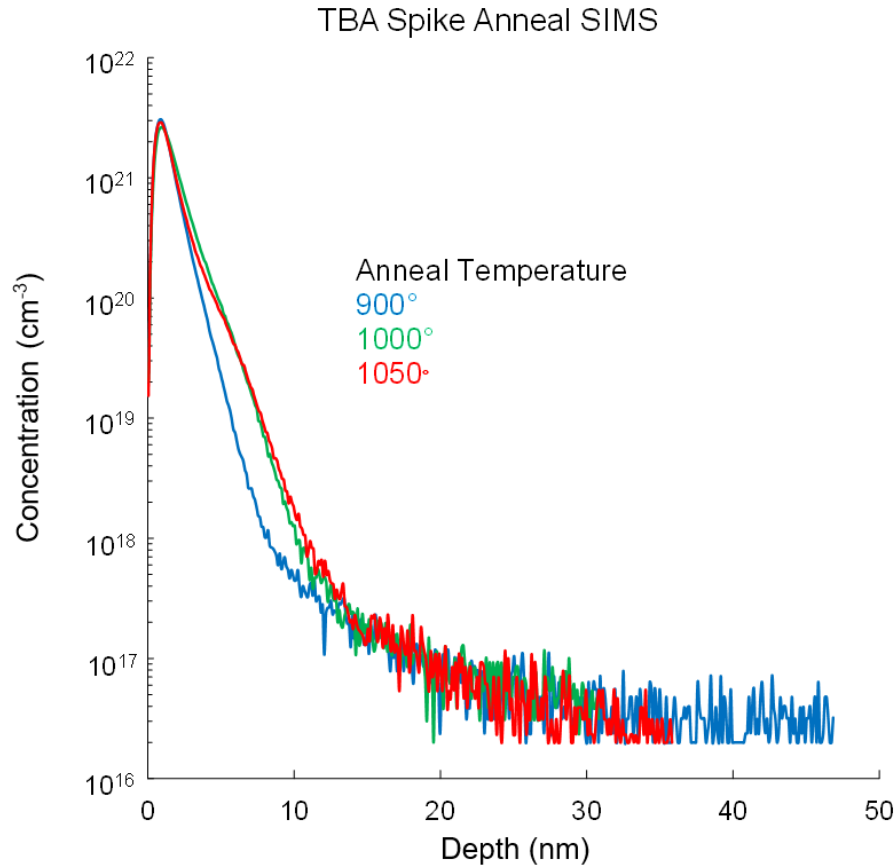


Figure 7: Spike Anneal performed on planer silicon substrates doped using optimised TBA process. 1000°C and 1050°C show similar greater levels on in diffusion compared with the 900°C anneal. Overall this process limits the in diffusion when compared to conventional RTA as in Figure 2.

Due to the use of an RTA at Tyndall with relatively low ramp up and ramp down rates, the amount of As diffusion was ~100 nm in the previous experiment (see Figure 2). This might be considered too much for USJ applications. A preliminary exploration into the control of diffusion was then carried out, using the TBA process as before but with a different RTA tool, this one with >100°C/s ramp up capability. Shown in Figure 7 are the data for anneals at 900, 1000, and 1050°C, 0 s hold time RTA. It can be seen the diffusion is greatly reduced created USJs of < 20 nm. This result shows promise, and in future work should be explored in greater detail in order to characterise fully and optimise the entire process flow.

2.4 CONCLUSIONS

In this work we investigated TBA as an alternative doping source for damage-free conformal doping of thin Si films and 3D device structures. Using an optimised process high levels of active As doping concentrations (close to 10^{20} cm^{-3}) were achieved in functional 3D devices, and could be further optimised by applying a spike-RTA demonstrated on planer silicon. For the optimised doping process, no evidence was observed of damage to the crystal structure, either internally in the wire or externally on the surfaces, which makes this technique compatible with GAA device architectures. An approximately 4 nm arsenic containing oxide layer was observed on the Si test structures, conformal to all 4 surfaces on substrate-released nanowires, and it is thought to be linked to exposure to the ambient.

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Chapter 3: ONE STEP LOW LOW-TEMPERATURE DAMAGE FREE DOPANT ACTIVATION OF THIN THIN- FILM SILICON DEVICES

3.1 INTRODUCTION

Ultra-shallow, high activation implantation is a key step to produce modern semiconductor devices. Ion implant is still the most widely used method for introducing dopant atoms due to it being well understood, very controlled, and has a high level of adjustment to control dopant concentration and depth.

A disadvantage of this method is the damage it causes to the silicon lattice along with the need for a high temperature anneal not compatible with some modern semiconductor materials. The process is also complex in comparison with some other doping technologies such as SOD and MLD.

In this chapter a method of low temperature activation of dopants by dynamic annealing during implant is discussed. This allows us to activate high levels of dopant at a significantly reduced temperature and without the need for the additional processing necessity of a high temperature anneal.

While the dopant implantation and activation in silicon is highly investigated, most of the work conducted focuses on optimising the traditional high temperature annealing step. With the goal of achieving USJs in mind the strategy has therefore been to decrease the thermal budget by means of shortening the time at these high temperatures and using unique methods to suppress transient-enhanced diffusion. Classical experiments conducted when information about silicon annealing was less understood investigated activation at lower temperatures^{82,83}. This work shown in Figure 1 demonstrates high levels of activation for both boron and phosphorous at lower temperatures. However, the phosphorous fraction active dose increases with implanted dose suggesting that the amorphous to crystalline transition enables its activation. However, boron has shown the opposite behavior, where high doses were substantially harder to activate at low temperatures suggesting it activates in a different manner to phosphorus.

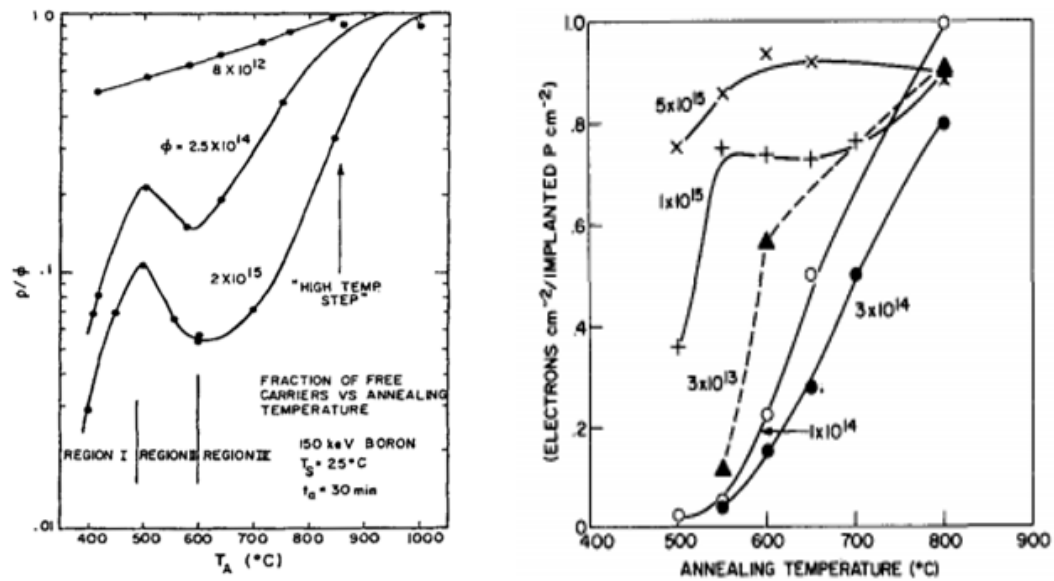


Figure 1 Activation of boron (left) and phosphorus (right) as a function of annealing temperature and implanted dose at substandard temperatures. Y axis in each case is active dose/implanted dose (activation percentage).

Low temperature doping would enable flexibility in the doping process to be applied after gate patterning. Currently in industry gate last processing is common as the materials used for high-k gate dielectrics are not temperature stable⁸⁴ and would not hold up under high temperature RTA normally needed for post implantation activation.

Low temperature doping is also important for applications outside of GAA silicon transistors. One of the major hurdles for the adaptation of low cost substrates for the use in thin film transistors or alternative non mono-crystalline silicon based solar cells is the high temperature anneal necessary to activate the dopants^{85,86}. Many of these applications do not need the same levels of supersaturation of dopants as is necessary for modern singles of nanometre transistors⁸⁷.

3.2 EXPERIMENTAL

3.2.1 Proof of concept results

Seen in Figure 2 is earlier work completed to benchmark doping processes for use in thin body SOI devices. Relatively simple SOI devices were used in this study to get benchmark results for various doping processes. The doping processes that were most successful could then be applied to the more industrial pertinent nanowire devices. The knowledge of the dopant activation from the less complex SOI devices could then be used to troubleshoot other nanowire electrical issues, such as contacting, or device structural failure.

The TBA process results shown, were using the technique described in chapter 2. The samples were preprocessed by degreasing in acetone and IPA, and then HF etched to remove the native oxide. The samples were then placed in a MOVPE chamber where TBA containing gas was flowed over them. This run of the process was the first onto 3D devices and the deposition of the layer shown in Chapter 2 Figure 6 was not expected. This insulating As_xO_y layer between the silicon and the contacts caused high contact resistance. The vapour MLD process involved placing similarly preprocessed SOI samples in vapours of a common MLD molecule, ADP (allyldiphenylphosphine). This process was used as opposed to standard liquid MLD as the vapour has a theoretically better chance of accessing nanowires devices likely leading to higher doping levels. The arsine process was described in previous work⁸⁸, it was similar to the TBA process but involved the use of a smaller arsine molecule which was thought to release more atomic H, believed to have caused the damage to the silicon film. The 450°C and RT implant samples were implanted with 2 keV phosphorus with a dose of $1 \times 10^{15} \text{ cm}^{-2}$. The difference in these samples was that the 450°C sample was implanted while the sample was kept at 450°C, to avoid amorphization by dynamic annealing, while the RT sample was implanted at room temperature and likely amorphised. All samples received the same 1050°C 5 second RTA.

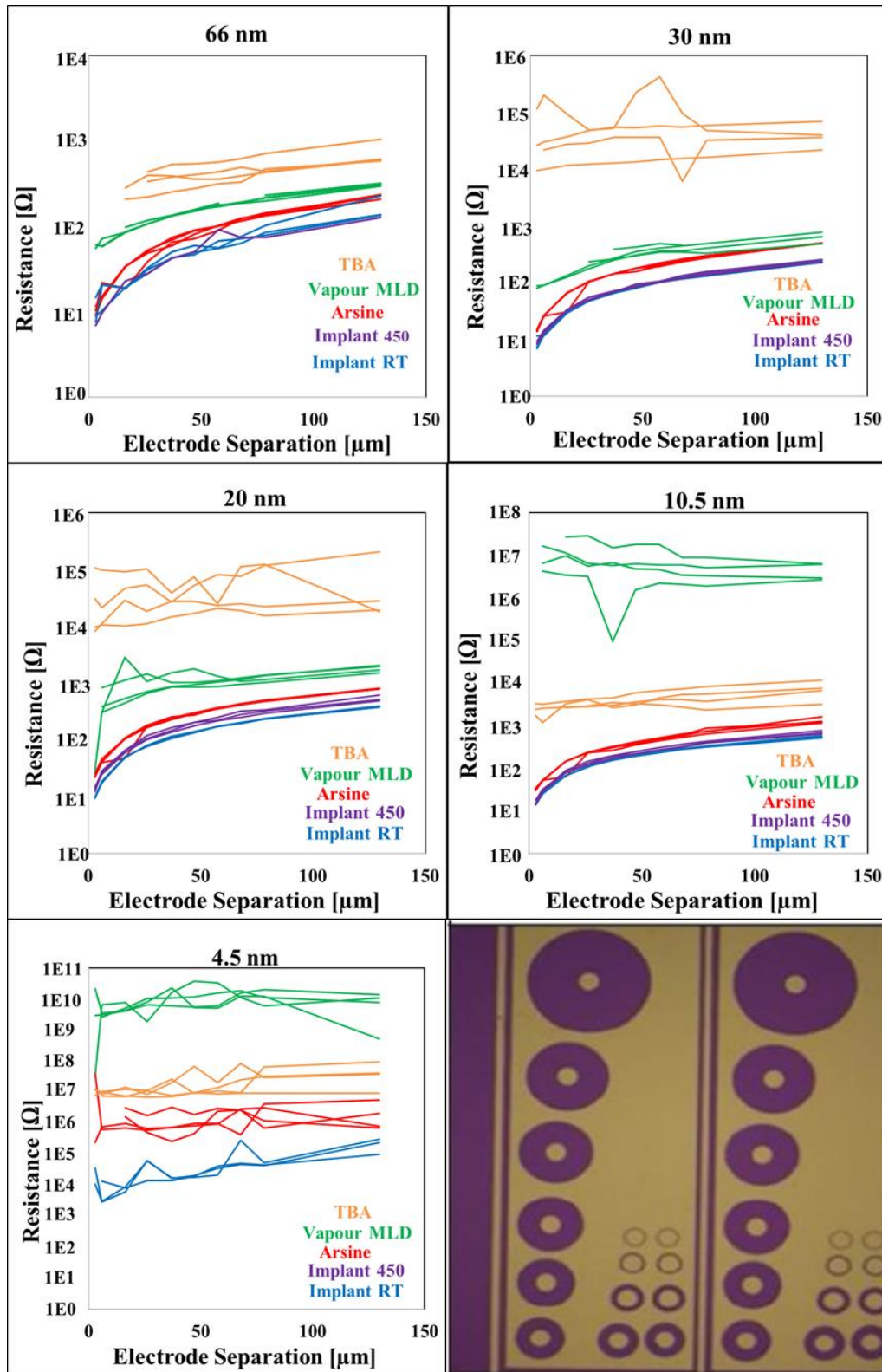


Figure 2 Earlier work performed benchmarking various process for use on GAA devices.⁸⁹ Bottom right image shows optical micrograph of CTLM devices used in this study. A two probe setup was used where the large rectangular gold area was used as one probe location and the other probe was the centre of each circle.

At that stage carrier profiling was carried out on selected samples *prior to any RTA*. While it was seen that after the 1050°C anneal there was no discernible difference to levels of dopant activation from the RT and 450°C samples, before annealing the 450°C showed very high levels of activation uncharacteristic of a standard anneal at 450°C, as seen in Figure 3. This was a surprising result as we did not expect a high level of activation in the as received sample (“As Rec” = no anneal post ion implant).

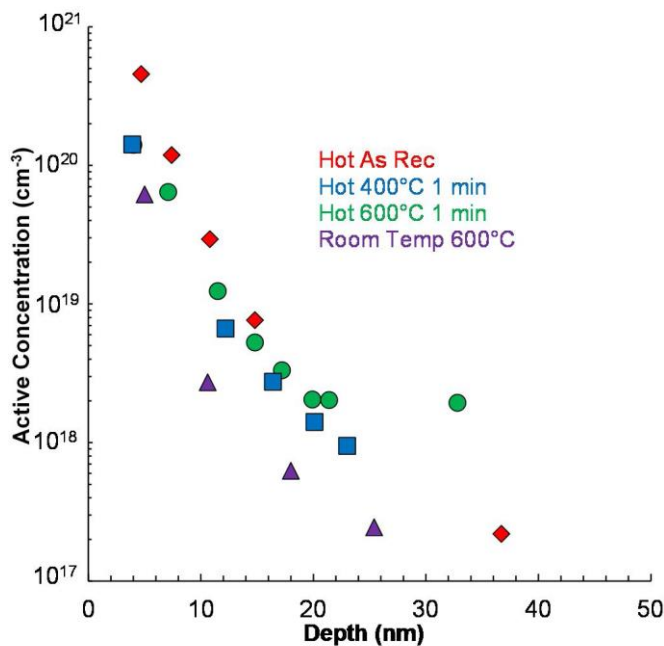


Figure 3 ECV profile of the proof-of-concept experiment. 2 keV phosphorus implanted samples hot sample was implanted at 450°C. Select samples were subjected to annealing at 400°C and 600°C for 1 min. For comparison room temperature implanted samples were also subjected to the same anneals.

	As Received	400°C 1 Min	600°C 1 Min
Heated Implant	35%	12%	11%
Room Temperature Implant	-	-	5%

Figure 4 Percentage activation of both room temperature and heated implant at various conditions. Percentage activation was calculated by integrating the ECV profile to calculate active dose and comparing this to the implanted dose of 1×10^{15} atoms/cm².

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It was theorised that this dopant activation before annealing was a potentially metastable state caused by incorporation during the dynamic recrystallization of the silicon during implant under temperature. Therefore, to test the stability of this state the chips were subjected to a 400°C and 600°C anneal for 1 min and ECV profiling repeated. 400°C and 600°C anneals showed similar substantial deactivation of the carriers as seen by ECV profiling. The room temperature implanted sample also exposed to these anneals as a control still had lower levels of activation at 600°C than that of the heated implant suggesting the higher level of activation was not completely eliminated. These high levels of activation were not seen in the electrical testing. This may be due to a limitation of the ECV. In the TEM images we see there is a high concentration of defects. ECV has been shown in previous work to struggle differentiating active dopants and defects⁹⁰. It is also possible that the level of activation is correct and that the high resistance from electrical testing is due to poor mobility rather than poor activation. Based on these results another experiment was planned where the temperature of the samples that were implanted was varied and compared. A 10 keV P2+ implant with a dose of $5 \times 10^{14} \text{ cm}^{-2}$ was used comparable to a 5 keV P implant at a dose of $1 \times 10^{15} \text{ cm}^{-2}$. Electrical characterisation was performed on SOI doped under each condition.

3.3 RESULTS AND DISCUSSION

3.3.1 Systematic experiment with ion implant temperature as variable

If dopants activate already during hot implantation, without the need for a post-RTA or flash or laser anneal, this would significantly reduce the thermal budget for device integration. This would also open up possibilities for back-end-of-line processing in the future, which enables 3D stacked integration of devices at different levels.

We had preliminary carrier profiling and electrical device data that suggests P is activated directly after hot implantation in Si, without a post-RTA or flash or laser anneal. However, that is just for one implant condition, so we wish to follow that up with a more systematic experiment in order to prove the validity of that result.

Beam-line ion implant 5 keV P with a dose to 1×10^{15} atoms/cm², with the chuck temperature as the variable was used for this experiment. To avoid overdoing the requirement on beam time, we proposed 5 different chuck temperatures as the variable, while keeping others constant. The samples are bulk (100) Si for ECV carrier profiling, and SOI for Transfer Length Method devices. The Si thickness in the SOI is varied, but all these samples were 1 cm × 1 cm, so many samples could be put in the ion implant chamber at the same time.

The experimental conditions are shown in Table 1 below.

material	size	ion species	energy (keV)	fluence (cm ⁻²)	Temperature (°C)	tilt angle (°)	twist angle (°)
Si	Several 1 cm × 1 cm samples	P	5	1×10 ¹⁵	Room Temp.	7	27
Si	Several 1 cm × 1 cm samples	P	5	1×10 ¹⁵	200	7	27
Si	Several 1 cm × 1 cm samples	P	5	1×10 ¹⁵	300	7	27
Si	Several 1 cm × 1 cm samples	P	5	1×10 ¹⁵	400	7	27
Si	Several 1 cm × 1 cm samples	P	5	1×10 ¹⁵	500	7	27

Table 1: Ion implantation / irradiation conditions relevant to experiment.

Shown in Figure 5 are the results of the experiment where samples were implanted at varied temperatures and compared for levels of activation. Samples dynamically annealed at temperature 200°C and below showed no activation. Activation levels increased proportionally with temperature within the values used for this experiment. The incomplete recrystallization and therefore incomplete doping during recrystallization are one possible explanation for the decreased levels of dopant incorporation. In the TEM images of Figures 9 and 10 it can be seen the 500°C sample is fully recrystallized while the 200°C remains polycrystalline. It is known that the rate of recrystallization and therefore dopant activation depends on the temperature.⁹¹

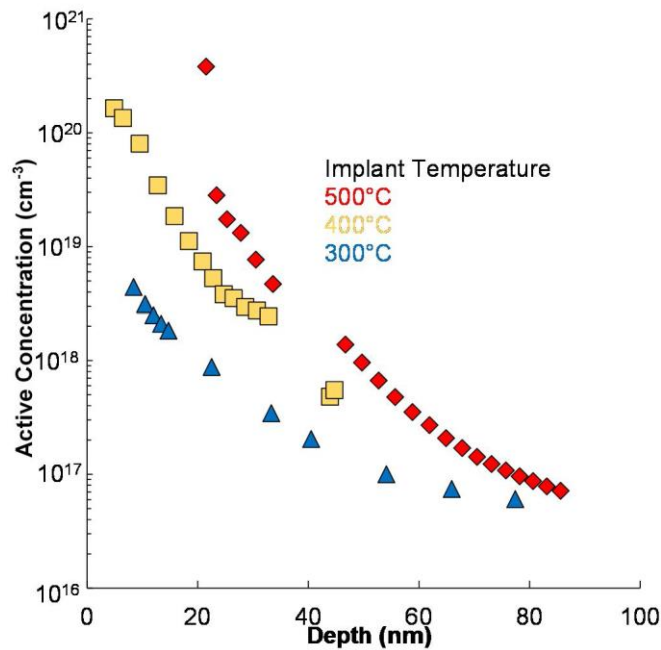


Figure 5 ECV profiles of silicon pieces implanted at various temperatures. Activation is proportional to implant temperature.

μ 4pp		Resistivity Measured in $\Omega \mu\text{m}$				
nm \ Temp		21	200	300	400	500
5		-	-	-	-	-
7		-	-	69.03	-	34.37
11		-	-	44.02	48.64	52.55
22		-	93.32	68.99	72.05	63.93
66		-	165.46	155.36	163.22	16.15

CTLM		Resistivity Measured in $\Omega \mu\text{m}$				
nm \ Temp		RT	200 °C	300 °C	400 °C	500 °C
5		-	-	-	-	-
7		-	-	72.60	312.00	-
11		-	59.20	45.80	45.20	-
22		870.00	67.60	73.40	70.80	67.50
66		940.00	154.00	143.00	143.00	151.00

Table 2 Shown here are the two sets of results obtained from implanting SOI films of various thicknesses at different temperatures without any activation anneal. The first set of results were obtained using μ 4pp. The second set of results are CTLM devices.

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Table 2 is two sets of results obtained from implanting SOI films of various thicknesses at different temperatures. The first set of results were obtained using $\mu 4pp$ directly onto the SOI chips of various thicknesses. Any absent values were attempted but resistance could not be measured accurately. The second set of results were from CTLM devices manufactured on various SOI thicknesses. The general increase of resistivity at 66 nm is likely due to shallow implant, meaning much of the 66 nm film would have lower levels of dopant incorporation. The sharp increase in resistivity at the lower thickness of 7nm and 5nm may be due to complete amorphisation of the silicon film during doping and therefore poor recrystallization. This poor recrystallization could cause degraded device resistivity due to the intrinsic property differences of silicon and polysilicon and also retardation of the recrystallization induced doping due to different crystallisation mechanics.

Generally, the resistivity seen is not consistent with the levels of dopant incorporation seen through ECV profiling. This could be due to many effects such as ECV artefacts inflating dopant activation levels, incomplete doping due to the shallow implant, residual crystal defects that may not have received enough thermal budget to anneal out, degraded mobility, or different activation mechanics between bulk silicon and 3D thin SOI devices for example trapped carriers at Si/SiO₂ interface. 3D active carrier profiling such as SSRM could be used to determine if the dopants are ECV artefacts or if the dopant incorporation is different than that of bulk silicon, however SSRM relies on resistance measurement to profile dopants so crystal defects may also interfere with this. There is also the possibility that any artefacts inflating ECV profiling might also affect SSRM profiles. Pseudo-MOSFET analysis⁹² could potentially determine the mobility but once again it is difficult to rule out all influences on this analysis. Further analysis therefore while possible is not without issues. Regardless of the answer to the comparatively low resistivity this is the main property of interest when talking about dopant activation in

GAA transistors so unless it can be addressed the identification of the root cause could be of limited use.

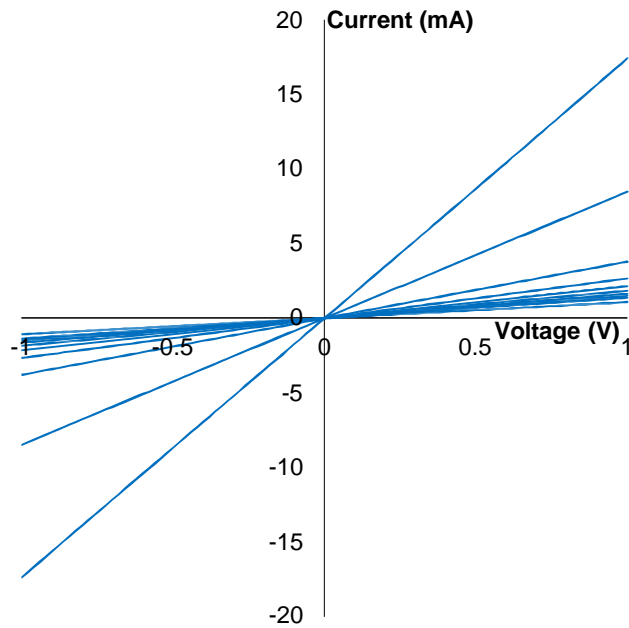


Figure 7 Representative I-V from the CTLM devices. Device behaved ohmically with low contact resistance. Each line represents a different electrode separation ranging from 130 to 3 μm .

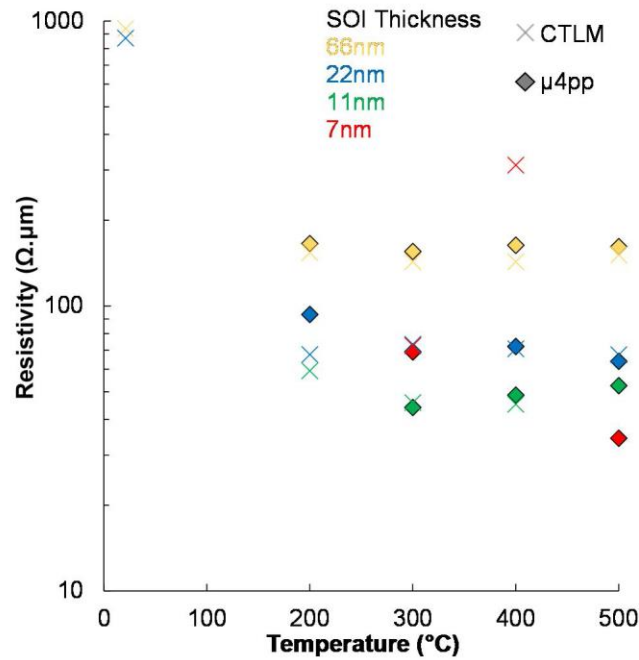


Figure 8 Electrical characterisation results plotted as temperature versus resistivity. Good agreement can be seen between $\mu 4pp$ and CTLM analysis.

TEM analysis was performed to get an understanding of the amount of damage left after dynamic annealing. XTEM of the 500°C implanted sample showed the presence of a crystal along with homogeneity of the silicon layer suggesting full recrystallization. Plan-view TEM imaging was performed and diffraction pattern obtained for the 200°C and 500°C implanted silicon. This confirmed that the 200°C sample remained polycrystalline while the 500°C sample had recrystallized under the higher thermal budget

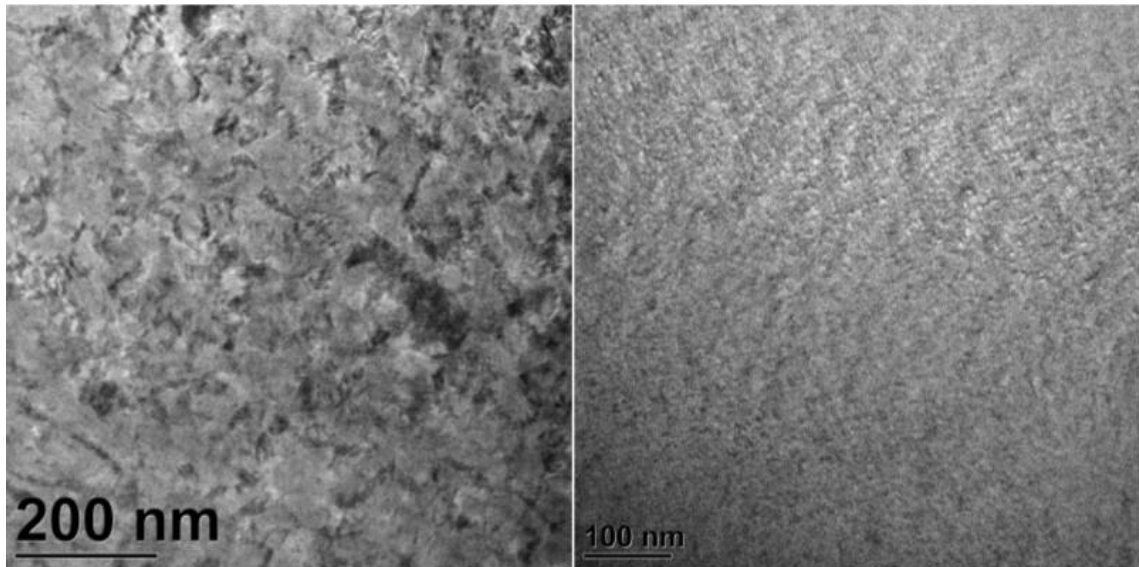


Figure 9 Plan-view TEM comparison of 200°C (left) and 500°C (right) implanted silicon. The 200°C silicon seems to be polycrystalline while the 500°C is fully recrystallized. This is confirmed in Figure 10 where the diffraction patterns can be seen for each case.

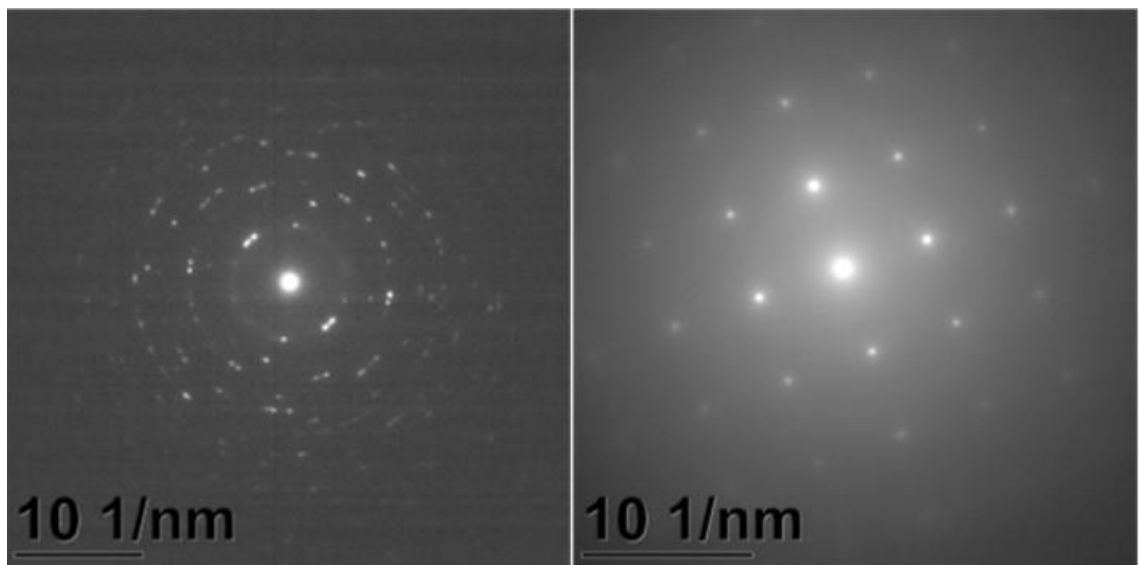


Figure 10 Diffraction pattern obtained from TEM of 200°C (left) and 500°C (right) implanted silicon. This confirms that the 200°C sample remains polycrystalline while the 500°C sample has recrystallized.

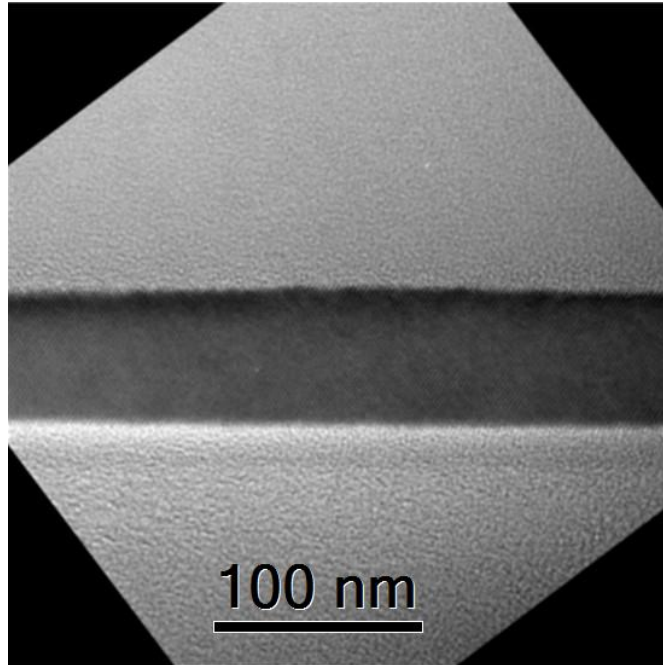


Figure 11 XTEM of 500°C implanted sample. The crystal lattice can be seen along with homogeneity of the silicon layer.

3.4 CONCLUSION

One step doping of silicon was achieved by means of implantation and dynamic annealing. This process was seen to be damage free under certain circumstances. This process has applications anywhere the simplification of the doping process to one step could be advantageous and with some further research and improvement could be used to dope GAA transistors.

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Chapter 4: CONCLUSION

Continuation of scaling silicon transistors towards GAA devices will require novel doping processes.

Demonstrated in Chapter 2 gas phase doping is a promising candidate as it has a superior ability to conformally dope tight 3D architectures when compared to ion implantation. This process needs to be optimised to find a balance between the potential for these processes to etch on one hand and deposit potentially unwanted layers on the other. Further work currently ongoing to limit the thermal budget of these process will also play a critical role in their applications in modern semiconductor processing where temperature sensitive materials are ever more present.

Chapter 3 shows a one step process that simplifies traditional ion implantation while also displaying a possible route toward high levels of activation at lower temperatures. The electrical characterisation of these devices showed how this process would need further optimisation to reach conductivity levels required for GAA transistors.